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Origin of the Shunt Currents and Their Influence on the Ideality Factor (η) of a p-n Junction

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Abstract: It is our current belief that non-ideal nature of the current – voltage characteristics of a p-n junction is mainly caused by the contribution from generation – recombination currents. It was, however, recently reported in a gate-controlled diode experiment that the ideality factor of a Mercury Cadmium Telluride junction diode exhibits strong dependence on the surface leakage current of the diode, which means that the surface leakage currents are another possible source that may be responsible for the non-ideal I – V characteristics of a junction diode. This work presents a general physical model that provides an insight in to the origin of the shunt currents in a p-n junction as the surface leakage currents are known to be modelled as shunt current. The role of surface leakage currents in influencing the ideality factor of the junction as one of the sources of shunt current therefore constitutes the main theme of the present communication. The investigation of the effect of dislocations, which also contribute to the shunt current, on the ideality factor of the junction is proposed to be a problem for future study. It is concluded that the surface leakage currents owing their origin to recombination currents are responsible for the operation of a shunt resistance in parallel to the junction and consequent degradation in its dynamic impedance. Whereas the previously reported increase in the thermal reverse bias saturation diffusion current of the junction diode is shown to be due to the real time transfer of minority carriers from the one side of the junction to the opposite side. But the degradation in dynamic impedance of the junction is due to apparent reduction in junction barrier hight from exp (qV/kT) to exp (qV/ηkT) by virtue of the operation of the shunt resistance in parallel to the junction impedance.

Keywords: Ideality Factor, p-n Junction, Semiconductor Diode, Shunt Currents, Surface Leakage Currents

1. Introduction

Surface leakage currents are among the known sources of shunt currents in a p-n junction. It was recently reported [1] during a study of modelling of current – voltage (I – V) characteristics of a mid-wave Mercury Cadmium Telluride photodiode in a gate-controlled diode experiment that the ideality factor of the diode is near to its value of unity for an ideal diode when surface potential of the diode has its optimum value corresponding to the minimal surface leakage current. Deviations of the surface potential from its optimum value results in non-ideal I-V characteristics. The ideality factor η of the diode exhibits an increasing trend with the increase of surface leakage current. Values of the ideality factor exceeding 2 were reported for very high surface leakage currents. The previous work [1] was more focussed towards the investigation of current transport mechanisms and therefore an important aspect namely the physical connection of surface leakage currents with the ideality factor of the junction diode got overlooked. The aim of the present work is to propose a physical model that provides more insight in to the origin of surface leakage current as shunt current and its further role in influencing the ideality factor of the p-n junction.

2. Physical Model

The transport of the current in an ideal p-n junction is described by the following well known Shockley's equation,

$$I_{dif} = I_{\mathrm{Sat}}\left[\exp\left(\frac{qV}{kT}\right) - 1\right] \quad (1)$$

Where I_{Sat} is the thermal saturation current of the thermally diffused minority carriers in an ideal junction, whose value is a function of some of the material and junction parameters. The functional relationship of I_{Sat} with these parameters depending on the type of a junction diode, i.e. epitaxial or bulk, can be found out almost in all standard text books on the Physics of Semiconductor junction devices.

Equation (1) is essentially the solution of a 1-D differential equation for the diffusion of thermally generated minority carriers from the quasi-neutral n and p regions of the junction to the edge of its depletion region under dark conditions. The appearance of the exponential term in equation (1) is the result of applying the following boundary condition during the solution of the 1-D differential equation,

$$n_{no} = n_{po} \exp (qV/kT) \text{ and } p_{po} = p_{no} \exp (qV/kT) \qquad (2)$$

Equation (2) essentially means that the minority carriers n_{po} (electrons) on the p-side of the junction are in thermal equilibrium with the majority carriers n_{no} on the n-side of the junction and remain separated from each other by an exponential barrier, exp (qV/kT), at a given applied bias voltage V and temperature T. The same is true for the holes on the n-side of the junction.

Sah, Noyce and Shockley have reported [2] that the current – voltage (I – V) characteristics of some Semiconductor junctions were non-ideal as they do not follow the ideal equation (1). The forward current of a non-ideal I – V grow as exp (qV/η kT) in place of exp (qV/kT). Here η is the ideality factor of diode, whose value is more than unity in case of non-ideal junctions.

Figure 1 shows the modified schematic view of the gate – controlled diode used in the previously reported [1] experiment for the sake of completeness of the discussions in the present work. The boundary condition written above as equation (2) is applicable to an ideal junction of unity ideality factor when the gate voltage is optimum corresponding to the negligibly low surface leakage current. Ideally speaking surface leakage current should be nearly absent. As the gate voltage deviate from its optimum value, surface leakage current begins to increase due to enhanced recombination of carriers at the surface / passivant-semiconductor interface on the p-side of the junction shown in Figure 1. The enhanced recombination of carriers at the surface / passivant-semiconductor interface on the p-side can be maintained along with the normal minority carrier diffusion current, if the additional minority carriers over and above their thermal equilibrium value for an ideal junction become available on the p-side. This additional requirement of minority carriers on the p-side of the junction is met by the leakage of additional electrons (minority carriers for p-side) from n to the p-side of the junction. The principle of detailed balancing demands the leakage of an equal number of holes (minority carriers for n-side) from p-side to the n-side. The current consisting of leaking electrons and holes from one side of the junction to the opposite side is essentially the shunt current of the junction, which is conducted from one side to the other side of the junction either via the surface conduction or through the dislocations that intersect the junction [3]. The part of the current, which is conducted by surface conduction constitutes the surface leakage current and the current conducted through the dislocations is the contribution of dislocations to the shunt current. These two current contributions to the shunt current can't be distinguished from each other in a real time situation and are therefore modelled as one gross contribution.

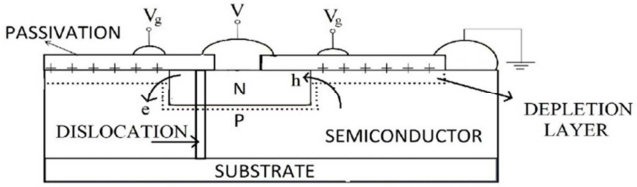

Figure 1. *Schematic side view of a gate-controlled diode structure.*

The model for conduction of shunt current via line dislocations has been already discussed in detail in ref. 3. The main objective of the present work is to discuss the physical model for conduction of shunt current via surface/interface path shown in Figure 1. It is well known that Semiconductor surfaces or passivant-Semiconductor interfaces contain space charge regions which contain fixed charges accompanied with either accumulation, depletion or inversion layer depending upon the sign of fixed charges and type of semiconductor and its surface potential underneath the passivation layer. Both accumulation and inversion layers are highly conducting. Whereas depletion layer exhibits a variable conductance depending upon the potential of the semiconductor surface [4]. The depletion layer shown in Figure 1 parallel to the p semiconductor surface beneath the passivation layer is the part of composite space charge layer whose conductance vary with the variation of semiconductor surface potential. The leakage of charged carriers (electrons and holes) constituting the surface leakage current takes place via this conducting layer and is shown by arrows in Figure 1. It will be worthwhile to mention here that the depletion region of the p-n junction away from the surface of semiconductor has no role in the leakage of charged carriers due to unfavourable energy barrier at the junction. In a gate-controlled diode the variation in the gate voltage controls the surface leakage current by modulating the conductance of the composite layer under the gate electrode. In a normal diode without gate electrode the magnitude of the surface leakage / shunt current is principally dependent on the magnitude of recombination current, I_R. The shunt resistance, R_S associated with the process of leakage of electrons and holes from one side of the junction to the other side is well described [3, 5] by the following relation,

$$R_S = \frac{kT}{qI_R} \qquad (3)$$

The shunt resistance, R_S operating in parallel to the junction impedance is dependent on the recombination current, I_R. Higher recombination currents requiring the leakage of relatively larger number of charge carriers

(electrons and holes) will result in relatively lower shunt resistance. Alternatively, both the recombination current I_R and the associated shunt resistance R_S can be made to vary by exercising control over the leakage of charged carriers / surface leakage current through gate electrode as already discussed above.

In the past shunt resistance calculations based on the relation (3) have been found to provide an excellent description of the variations in the zero-bias resistance-area product, quantum efficiency, spectral response and minority carrier life time as a function of dislocation density and operating temperature in Mercury Cadmium Telluride junctions [3, 5-10].

In a gate-controlled diode experiment the availability of additional minority carriers, electrons on the p-side and holes on the n-side, as a consequence of change in surface leakage current disturb the equilibrium of minority carriers represented by equation (2) on the two sides of the junction. Let us now re-write equation (2) for this new situation in which the minority carriers in the quasi-neutral n and p regions of the junction have increased with the change of gate voltage and the consequent increase of surface leakage current. The modified version of equation (2) in this changed situation may be re-written as follows,

$$n_{no} = (n_{po} + \Delta n_{po}) \exp (qV/\eta\, kT) \text{ and } p_{po} = (p_{no} + \Delta p_{no}) \exp(qV/\eta kT) \quad (4)$$

In equation (4) Δn_{po} and Δp_{no} are equal in number and respectively represent the number of additional electrons and holes that leaked to the p and n side of the junction with the variation of gate voltage / surface leakage current. It may be noted from a comparison of equations (2) and (4) that the number of majority carriers on the n and p side of the junctions have their nearly original values, i.e., independent of the gate voltage. Thus, to compensate for the increased number of minority carriers in the pre-exponential factor, the ideality factor η is to be inserted in the denominator of the exponential term and should have a value of more than unity. In a general case if equation (4) is used as boundary condition in place of equation (2) to be able to include the effect of variation of surface leakage currents, then the resulting Shockley equation for the diffusion of carriers to the junction will be as follows,

$$I_{dif} = I'_{Sat} \left[\exp\left(\frac{qV}{\eta kT}\right) - 1\right] \quad (5)$$

Above equation shows that the presence of shunt currents can also be one of the sources of non-ideal behaviour of the forward I – V characteristics with relatively higher reverse bias saturation current of diffused carriers in a p-n junction.

3. Discussions

As already discussed in the preceding section, the surface leakage currents owing their origin to recombination currents are responsible for the operation of a shunt resistance in parallel to the junction and consequent degradation in its dynamic impedance. This conclusion is fully consistent with the experimental observation (e.g., refer to figure on page 084508-7 of ref. 1) of degradation of dynamic impedance of the diode with increasing surface leakage current. Further the prediction of the above presented physical picture in regard to increase in thermal saturation current I'_{Sat} of the diffused charge carriers with the increase of surface leakage currents is also fully consistent with the previously reported results (see the figure on page 084508-9 of ref.1) that show an increase in thermal saturation current of the diode with the increasing surface leakage current. Here it is important to note that the increase in the reverse bias saturation current of diffused carriers is due to the real time transfer of electrons and holes from one side of the junction to the opposite side via shunt current path. But the degradation in dynamic impedance of the junction is due to apparent reduction in junction barrier hight by virtue of the operation of the shunt resistance in parallel to the junction impedance.

Above, the role of surface leakage currents has been mainly discussed as the surface leakage currents vary with the variation of gate voltage. In a practical case, leakage of electrons and holes from one side to the other side of the junction can also take place through the line dislocation that intersect the junction. A line dislocation crossing the junction is shown in Figure 1 to indicate the additional shunt current path. Though the effect of line dislocations on the dynamic impedance of the junction is practically well known [3, 5-12] but the direct evidence of their influence on the ideality factor of the junction remains unknown. In case of shunt current contribution due to dislocations the ideality factor of the junction is likely to exhibit its dependence on dislocation density. It is therefore suggested as a problem for future investigations. However, an increase in the ideality factor of type II InAs/GaSb diodes with the decreasing temperature has been already reported [13] and interpreted due to the increasing effect of dislocations due to the diminishing screening effect of intrinsic carrier concentration with the reduction of temperature.

4. Conclusions

In summary it can be said that the presence of recombination currents in a junction are responsible for giving rise to the shunt currents. Among the primary sources of recombination currents are the defects and dislocations which may be present either at surfaces or passivant-semiconductor interfaces or in the quasi-neutral n and p regions of the junction material. The current consisting of leaking electrons and holes from one side of the junction to the opposite side constitute the shunt current. The shunt current conducted via surface or semiconductor-passivant interface conduction is the surface leakage current and the shunt current conducted via dislocations that cross the junction is the dislocation contribution. Shunt currents degrade the dynamic impedance of the diode and are also

responsible for the non-ideal behaviour of the forward I – V characteristic of the junction as discussed in preceding sections.

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