**Journal of Electrical and Electronic Engineering**
2017; 5(5): 156-166
http://www.sciencepublishinggroup.com/j/jeee
doi: 10.11648/j.jeee.20170505.11
ISSN: 2329-1613 (Print); ISSN: 2329-1605 (Online)

# A Fault Tolerant Voter Circuit for Triple Modular Redundant System

**Mohammed Hadifur Rahman*, Shahida Rafique, Mohammad Shafiul Alam**

Department of Electrical and Electronic Engineering, University of Dhaka, Dhaka, Bangladesh

**Email address:**
hadifur@gmail.com (M. H. Rahman), msalam@du.ac.bd (M. S. Alam)
*Corresponding author

**To cite this article:**
Mohammed Hadifur Rahman, Shahida Rafique, Mohammad Shafiul Alam. A Fault Tolerant Voter Circuit for Triple Modular Redundant System. *Journal of Electrical and Electronic Engineering*. Vol. 5, No. 5, 2017, pp. 156-166. doi: 10.11648/j.jeee.20170505.11

**Received**: June 18, 2017; **Accepted**: June 28, 2017; **Published**: September 5, 2017

**Abstract:** Defect rate in Nanoelectronics is much higher than conventional CMOS circuits. Hardware redundancy can be a suitable solution for fault tolerance in nano level. A voter circuit is a part of a redundancy based fault tolerant system that enables a system to continue operating properly in the event of one or more faults within its components. Robustness of the voter circuit defines the reliability of the fault tolerant system. This paper provides simulation results and analysis of a fault tolerant voter circuit. In a Triple Modular Redundant (TMR) system, the robustness of the voter circuit has been improved. For this purpose, redundancy at transistor level has been added. In this technique each transistor of the various building blocks (Ex-OR gate, Multiplexer) of the voter circuit is replaced by a quadded-transistor structure. Quadded transistor structure provides built in immunity to all single defects as well as a large number of multiple defects. To evaluate the effectiveness of the voter circuit an IC layout in 90nm CMOS technology is developed. FPNI layout using qNAND hypercell is also designed and analysed. By simulation procedure it has been shown that the proposed fault tolerant voter circuit works properly as a majority voter in different faulty conditions of a TMR system. Moreover, it has been shown that in the presence of internal hardware failure (failure in transistor level) the voter circuit works properly.

**Keywords:** Fault Tolerance, Triple Modular Redundancy, Voter Circuit, XOR Gate, Multiplexer

## 1. Introduction

In nano-electronics the method of fabrication is very diferent. Nano-electronics circuit is a regular structure generated by a stochastic self-assembly process. Stochastic self-assembly means that ICs will be fabricated with little or no outside intervention. Due to lack of outside intervention nano fabrication is more prone to defects. The exact level of defect densities is unknown, but it is assumed that 1-15% of the resources on a chip (wires, switches FETs etc) will be defective [10, 14].

Some fault tolerance techniques can handle both defects and transient faults through hardware redundancy. Defects are characterized on a statistical level instead of specifically mapped. For a given technique a given percentage of faults can be mitigated whenever they may occur. [18] determines a large rectangular region that is devoid of any such defects. Such a sub-crossbar region can be reliably used for mapping Boolean functions. In the work proposed by [19], they develops a complete synthesis and performance optimization methodology for switching nano-crossbar arrays that leads to the design and construction of an emerging nanocomputer. [20] introduces a new approach to design fault-se-cure encoder and decoder circuitry 8 for memory designs. The key novel contribution of this paper is identifying and defining a new class of error-correcting codes whose redundancy makes the design of fault-secure detectors (FSD) particularly simple.

### *1.1. Triple Modular Redundancy*

N-tuple modular redundancy (NMR) is an early idea by von Neumann for fault masking. In NMR each gate is duplicated N times (N is an odd number) and arbitration unit is used to decide the correct value based on majority. The final arbitration unit decides the reliability of such designs.

Triple Modular Redundancy (TMR) is a special case of NMR. TMR is based on hardware redundancy. In TMR, three identical modules perform the same operation. Outputs of these modules pass through a voter circuit. The voter produces the final output according to the majority inputs. If we further triplicate the TMR circuit, the obtained circuit will get nine copies of the basic module and there will be two layers of majority gates. This process can be repeated, which is called cascaded triple modular redundancy (CTMR) or recursive triple modular redundancy (RTMR).

Using CTMR in a nanochip with large nanoscale devices would require an extremely low device error rate [11]. In [12], it is shown that recursive voting leads to a double exponential decrease in a circuit's failure probability. But the problem is that a single error in the last majority gate can cause an incorrect result which will make the circuit less effective.

The use of TMR (Triple Modular Redundancy) and its variants are most commonly for SEU (Single Event Upset) mitigation [6, 7, 11]. The excessive area overhead is the main disadvantage of Triple Modular Redundancy (TMR). Specifically a design based on TMR occupies 200% more area than the original circuit. The Selective Triple Modular Redundancy (STMR) technique uses partial redundancy for SEU immunity [12]. The STMR technique operates on a gate-level circuit. At first the sensitive gates are identified and then only such gates are triplicated. But the LUT network obtained after the technology mapping stage, becomes very different from the gate-level circuit. After the technology mapping stage the area savings at the gate-level circuit are diminished. In Reduced TMR (RTMR) redundant copies of only a reduced set of LUTs are created. This reduced set of LUTs is first identified using an extension of a standard gate-level technique described in [12].

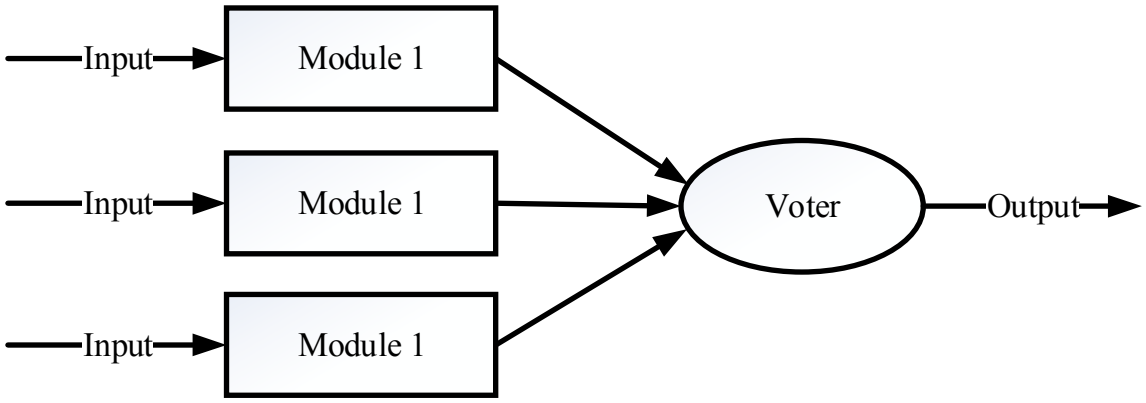


***Figure 1.*** *Triple Modular Redundancy.*

Even in the presence of high device failure or soft error rates in nanocomputing TMR technique provides high reliability despite the high redundancy overhead [13]. But the increment in reliability depends on an assumption that the voter block is free from the same failures that the rest of the design is facing. While this assumption seems true for traditional silicon technologies, it is very difficult for designs based on nanotechnology. The quadded-transistor technique can improve the reliability of Triple-Modular Redundancy by voter hardening [5].

### *1.2. Fault Tolerant Voter*

In NMR systems the reliability of the voter is very important in order to decide the final output. There are several voting strategies. These are majority, median or plurality [3]. At low redundancy factors ($N < 7$) the implementation of majority voter is more efficient [4]. The former research works are mainly based on the assumption that the voter is fault free [1], [2]. However, there are possibilities of faults in voter circuit also.

### *1.3. Different Voters*

*A. Classic Voter*

According to the boolean expression in (3), the classic voter circuit is shown in Figure 2(a). However, this structure immune from a single-fault only if it occurs on one module. But due to a failure of AND or OR gates, there is a possibility of incorrect outout. For example, if A = B = C = 0 and there is an unique fault in S1, the output will be V = 1 which is an incorrect value.

Another fault-tolerant voter circuit (NFTVC) [5] is shown in Figure 2(b). The circuit uses a priority encoder to produce the select signal for the multiplexer. With A = B = C = 0, if any of the nodes in the voter, i.e. either S1 or S2 is stuck to 1, the circuit will still produce the correct output as 0. This voter structure is fault-tolerant but not succinct.

if I1 = 0, then sel = 0 and A (equals to B) is going to be selected as the output;

if I2 = 0, then sel = 1 and C (equals to B) is the selected output.

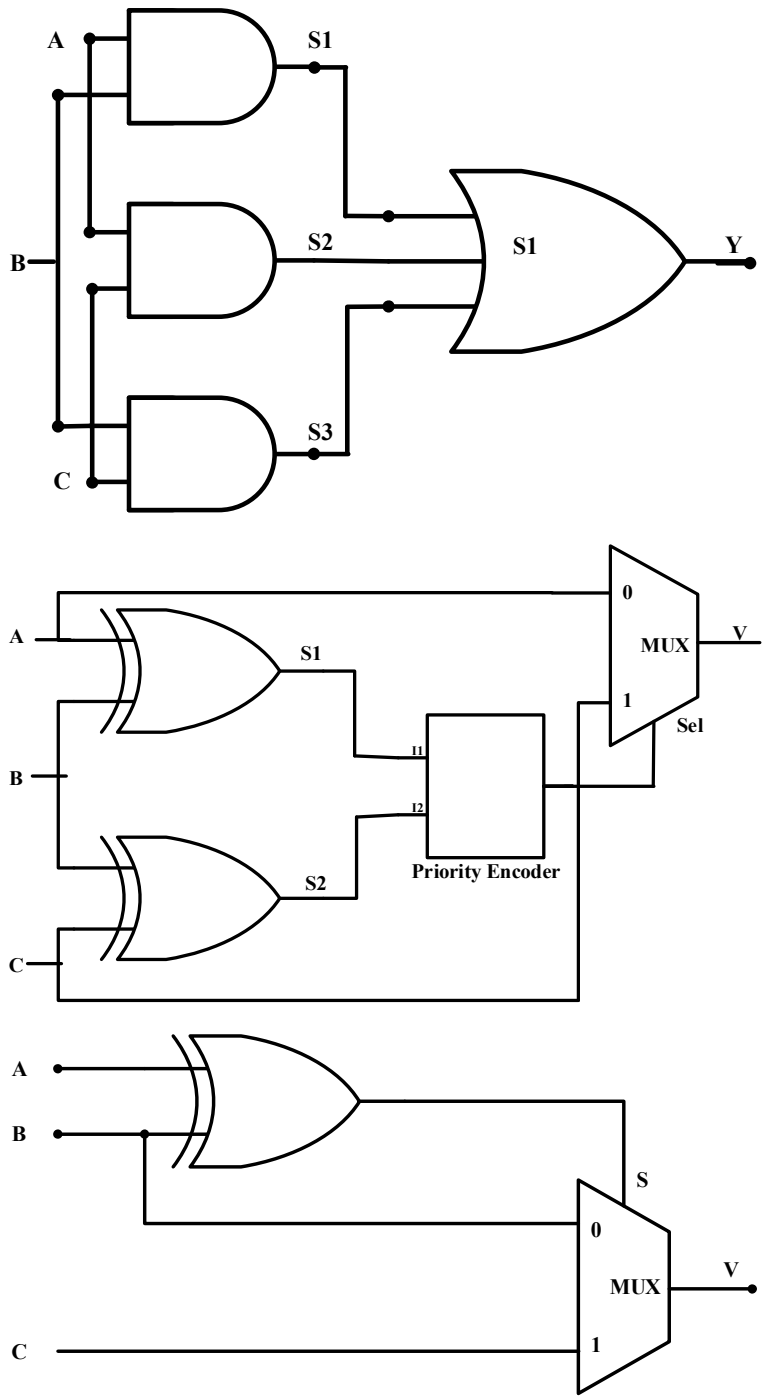


***Figure 2.*** *a) Conventional Scheme of a majority Voter b) Kshirasgar's scheme (NFTVC) of Majority Voter c) Fault Tolerant Voter proposed by Tian Ban.*

*B. A simple Fault Tolerant Voter*

In this work, an alternative scheme is followed for majority voting presented in Figure 4 as proposed in [6]. This structure is fault-tolerant following the analysis below:

*a) A fault occurs on the voter:* It means that the unique internal node S is stuck to a fault. Due to the single-fault model, the output is correct, independent of the value S (A =B = C)

*b) A fault occurs on one of the modules M:*

Case 1 (C is faulty): The logic signals A and B are the same and S = A⊕B. So, the multiplexer's output will be signal B which represents the majority value.

Case 2 (A or B is faulty): The logic signals A and B are different and the majority must be the logic value given by AC + BC, which corresponds to logic value C. According to the scheme, this relation is respected because S = A⊕B = 1.

### *1.4. Quaded Logic*

Quadded logic [10] is an adhoc configuration of the interwoven redundant logic which is a fault-tolerant technique introduced by Pierce [10]. In quadded circuit each NAND gate is replaced with a group of four NAND gates, each of which

has the twice as many inputs as the one it replaces. Then these four outputs of each group are divided into two sets of outputs, each providing inputs to two successive gates. In a quadded circuit the interconnections are eight times as many as those used in the non-redundant form. In a quadded circuit, a single critical error (1 – 0) can be corrected by passing through two stages of logic and a single sub-critical error (0 – 1) will be corrected after passing a single stage. It is very important that the interconnect pattern at the output of a stage is different from the interconnect patterns of any of its input variables. Though the quadded logic is an appropriate defect tolerance technique for most single errors, but the errors occurring at the last two stages of logic may not be corrected. Figure 2 shows an example of TMR and quadded logic circuits.

## 2. Methodology of Proposed Voter Circuit

This paper presents a promising fault tolerant technique for majority voter circuit used in TMR.

(a) A fault tolerant voter circuit from [6] has been chosen.
(b) Moreover to make the voter circuit more robust, a transistor level redundant technique is used. Using Quadded Transistor logic as described, a NAND gate is made.
(c) Each transistor of the NAND circuit is replaced with a quadded transistor structure. The schematic of this quadded structured NAND (qNANAD) gate and its block diagram is drawn by a commercial software DSCH, as shown in figure 4.
(d) Using this qNAND the schematic diagram of an Ex-OR gate (qEx-OR) and a multiplexor (qMUX)is drawn as shown in figure 5.
(e) Using these qEx-OR and qMUX circuit finally the schematic of desired voter circuit is made as shown in figure 5.
(f) From the schematic of the voter circuit, the Verilog code is obtained.
(g) Compiling the Verilog, IC layout of the proposed voter circuit is gained as shown in Figure 6.
(h) Then the spice simulation is performed in the environment of the Commercial software Microwind.

The proposed circuit is more robust because it is fault tolerant for a single fault in each quadded transistor structure. If there are more faults in different quadded transistor structure the circuit works properly. All possible faults are tested by simulation.

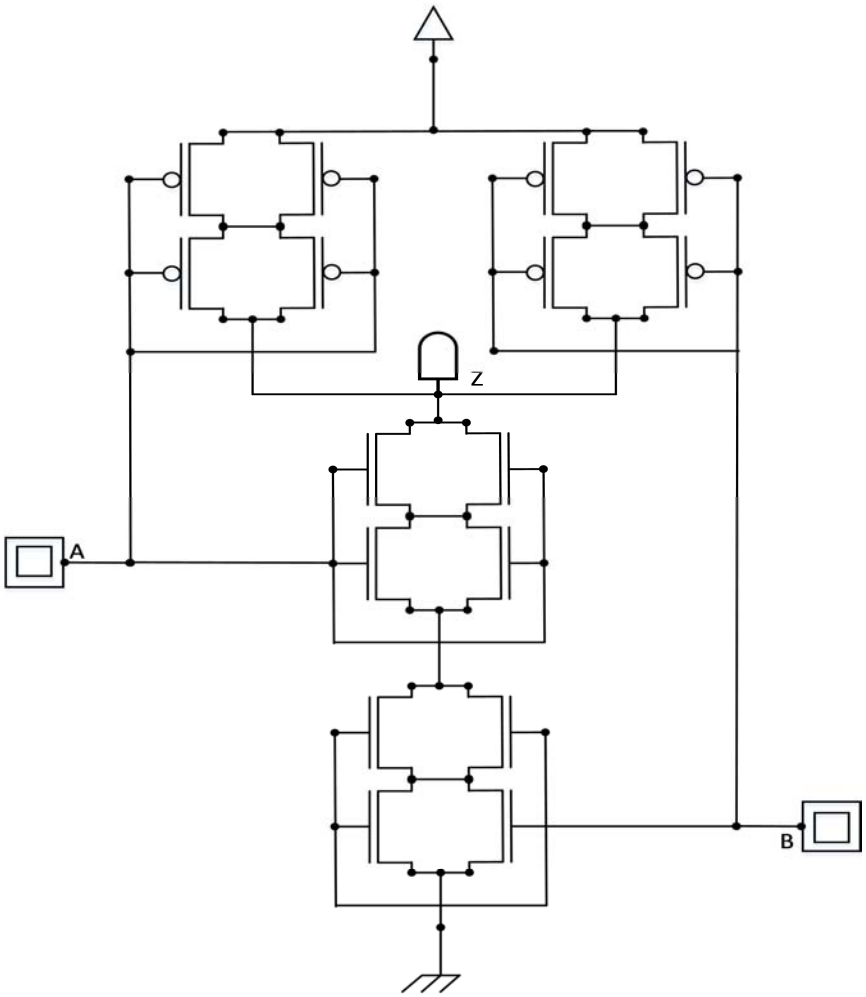


***Figure 3.*** *qNAND Schematic.*

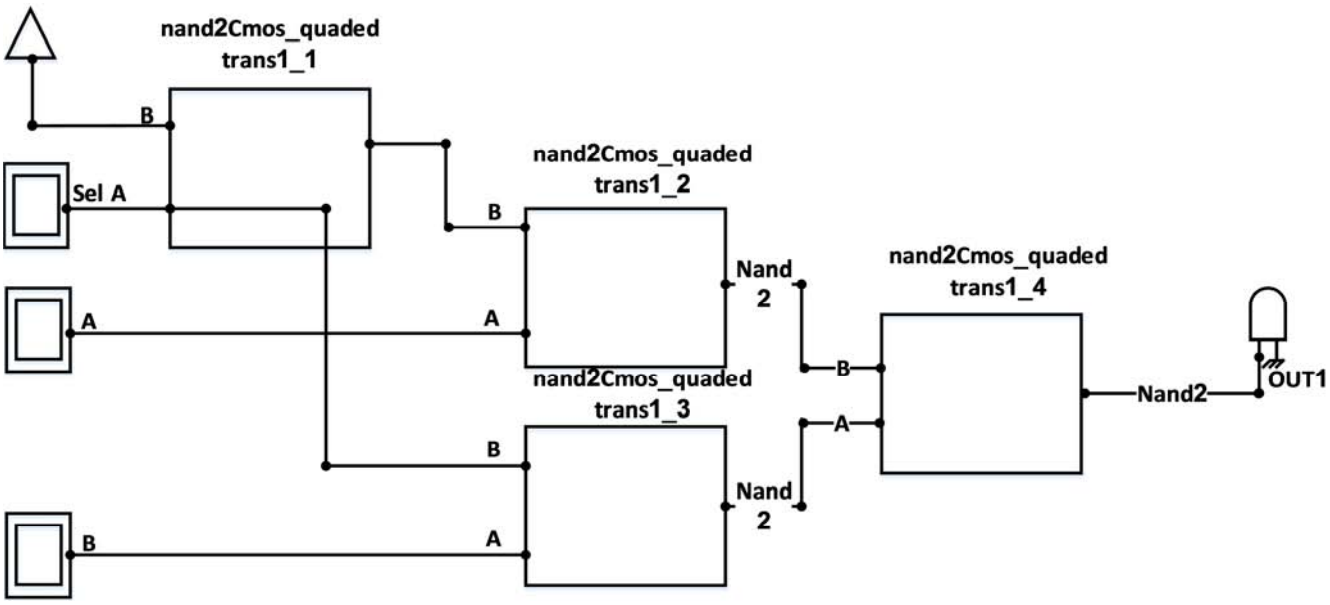


***Figure 4.*** *Schematic of qMUX.*

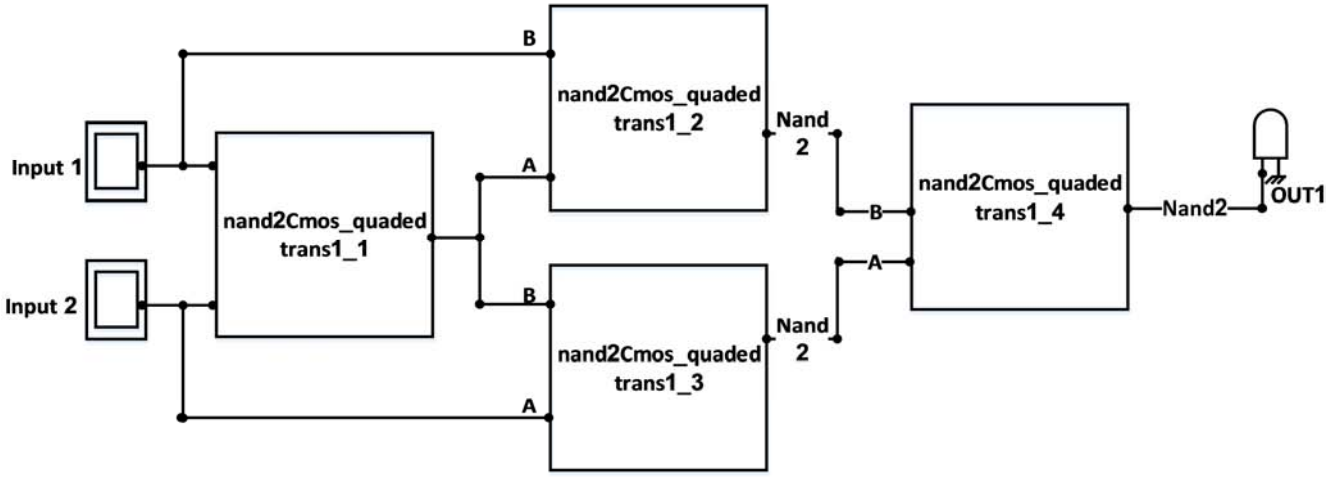


***Figure 5.*** *Schematic of qXOR.*

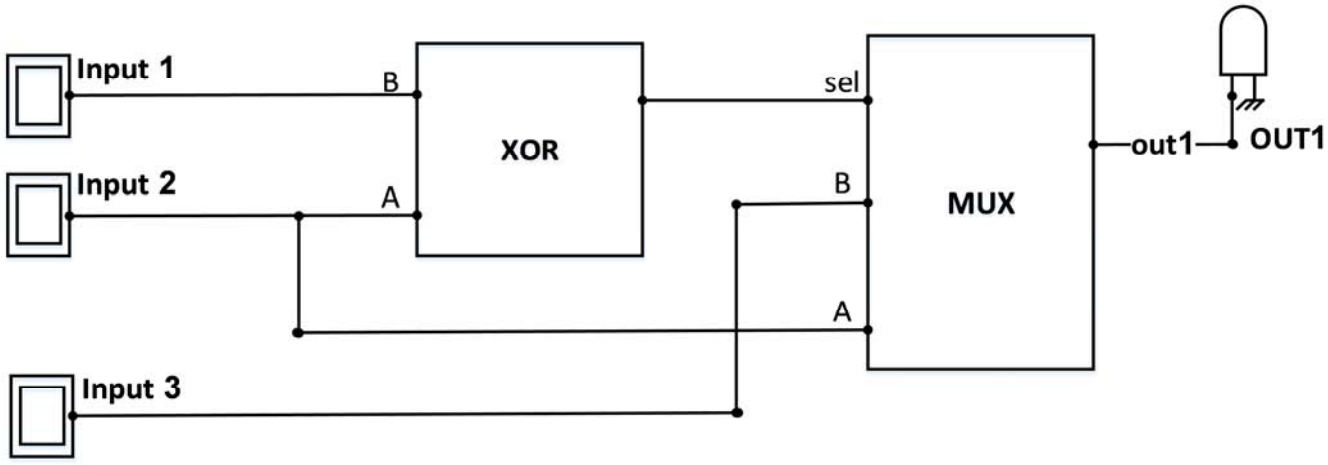


***Figure 6.*** *Proposed Voter Circuit.*

## 3. Simulation of Proposed Voter Circuit

To optimize the FPNI system for an intended application (voter Circuit), the hypercell is customised prior to fabrication. Snider and Williams in their original work [16], showed two types of hypercell.

A4×4 and hypercell consisting four two cell NAND gate eight single cell buffer gate.

A6×7 hypercell that provides a flipflop in addition to the first one.

An alternative 4×4 hypercell is used for this voter circut design. as shown figure 7. It consists of eight 2 input NAND gates only. For any intended applicatipon this hypercell can be customised using this universal gate.

Proposed reliable voter circuit consists of an XOR gate and a 2:1 multiplexer. As shown in figure 7, to realize the 2 input XOR gate , 4 NAND gates is configured (gate 1, 2, 3 and 4) and to realize the multiplexer rest of the four NAND gates of the hypercell were configured, combinedly realizing the voter circuit.

All the parts of the voter circuit can be specified precisely in the CMOS layout level with specific CMOS components. The FPNI layout for our design (voter circuit) is shown in figure 7. As shown in this layout, we used all the NAND gates in the hypercell which ensures maximum utilization of area. To facilitate the alignment of uniform nanowire interconnect structure the mapping of FPNI gates to integer unit cell can be inefficient. However, in designing the layout shown in figure functionality of the circuit was given more priority.

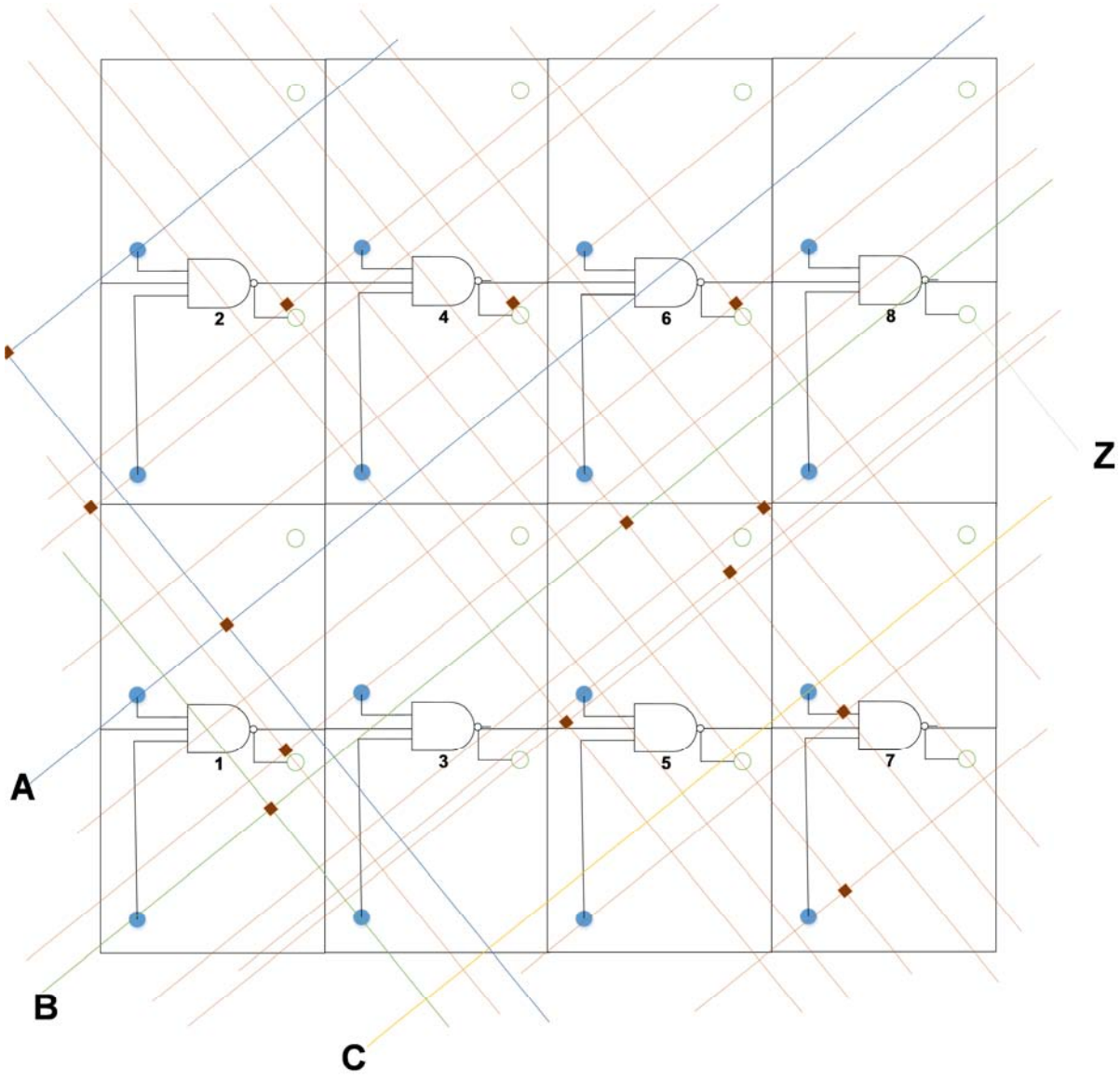


***Figure 7.*** *FPNI Voter Circuit Using qNAND.*

It is considered that, the voter circuit gets 3 inputs (in1, in2, in3) from the same source. So ideally the inputs should be same. Due to a fault if any one of these inputs does not follow the others, then the voter will make the output according to majority.

A simulation procedure is followed to establish the robustness of our proposed voter circuit. The effect of different faults are examined that may occur in a TMR system. These faulty situations are defined as different cases described below.

Input in1 is faulty. Its value is stuck or fixed to 0 state. But other inputs in2 and in3 are working properly and they are

following the original input. So in2 and in3 are following each other. The situation is described as shown in Figure 8 and Figure 9 as stated below.

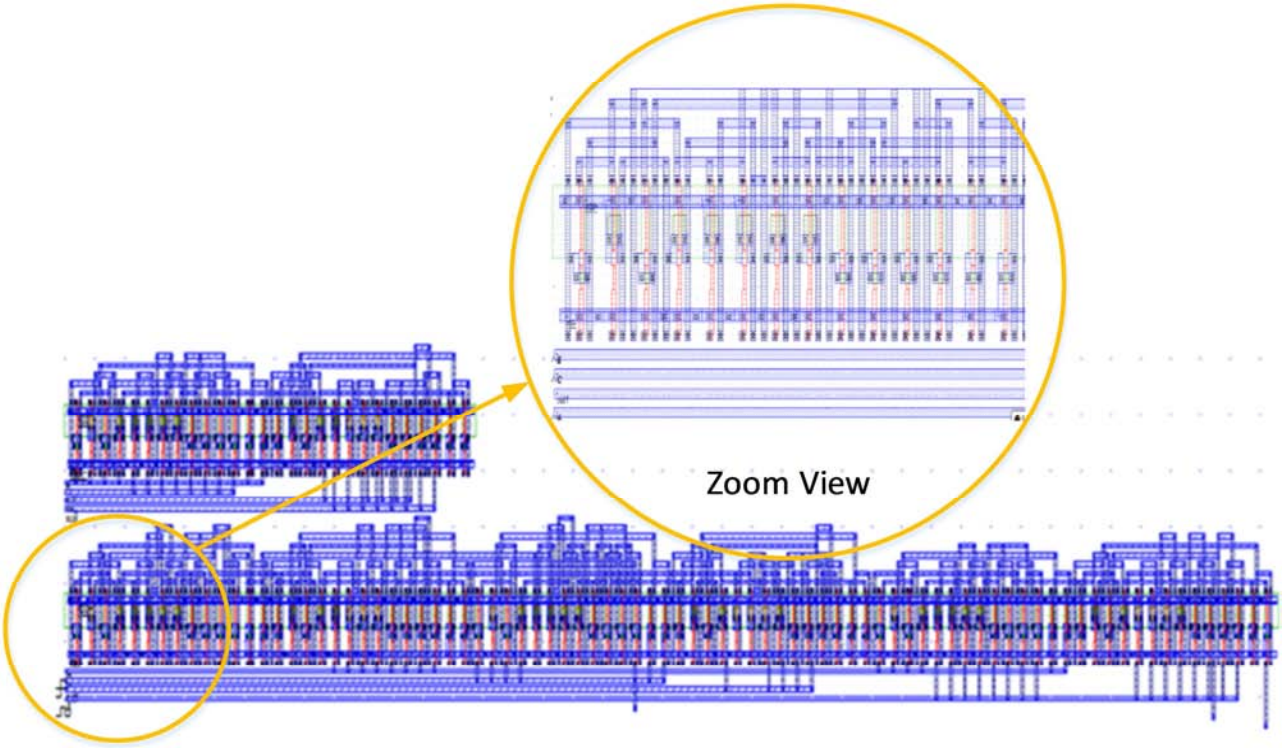


***Figure 8.*** *Layout of proposed Voter circuit.*

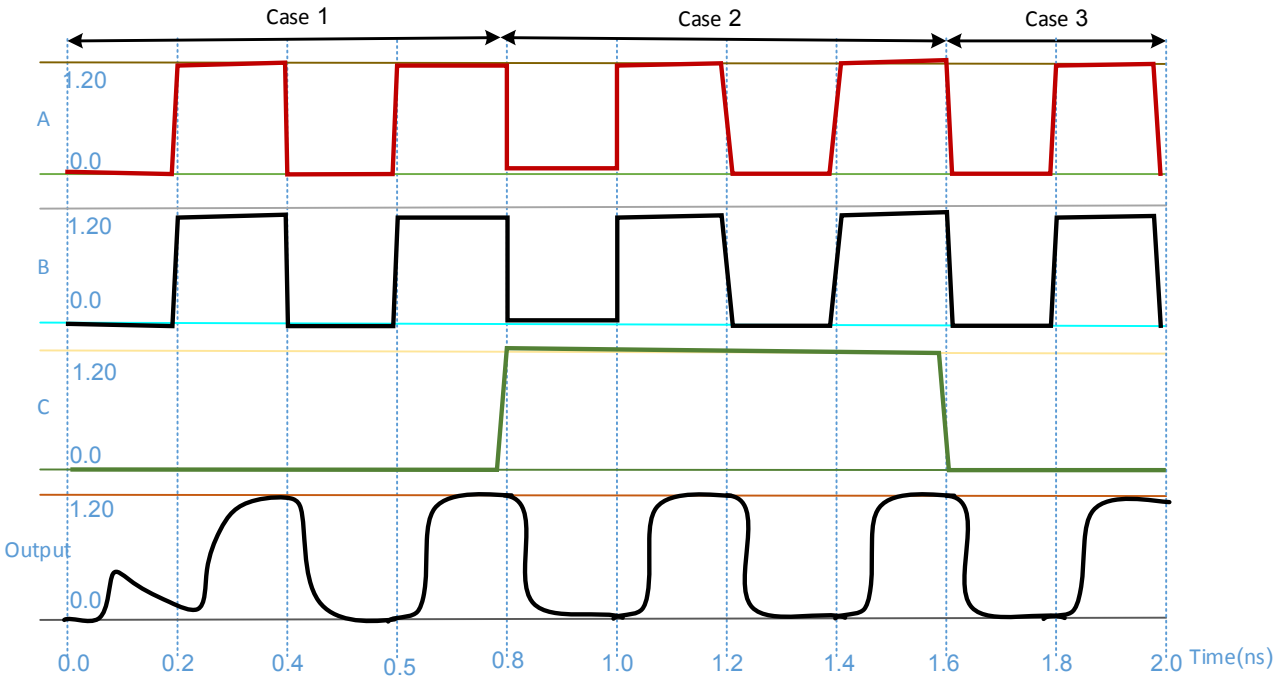


***Figure 9.*** *Simulation output of the proposed voter circuit.*

Case 1: C is stuck-at-0(s-a-0), A. follows B. So the output out1 follows A and B

Case 2: C is stuck-at-1(s-a-1), A. follows B. So the output out1 follows A and B.

Case 3: C is stuck-at-0(s-a-0), A. follows B. So the output out1 follows A and B.

## 4. Fault Injection

However, for making any circuit fault tolerant, redundancy

is an appropriate choice. In this paper, triple mudular redundancy has beed used for such purpose. As we know, a majority voter circuit is need for TMR system. But the voter circuit itself may be faulty. To resolve this problem, QNAND has been used for making multiplexer and XOR gate which are are the basic building block of Voter circuit. This fault tolerant tolerant voter circuit can perform properly inspite of hardware hardware defect in consisting QNAND. Again a majority voter circuit follows the majority of the input. If it works as like this, it's working properly otherwise it's not working properly. To asses the fault tolerance of proposed voter circuit, circuit, it is tested against different fault models models such uck at 0, stuck at 1, bridging fault modelas stodel

*Testing with stuck at fault 0*

Stuck at 0 is a basic fault model for testing performance of any design. In such cases, a particular elements are set to be open. As a result, the whole component fails to operate correctly. If the defects do not occur in any two parallel transistors, double stuck open or their corresponding bridge effects are tolerated. In the Figure 10, proposed voter circuit is is consists of faulty components, ahere stuck at 0 is applied. Its corresponding output is given in Figure 11, from where it is is seen that, for the case 1 output is following A and C where B B is stuck at 0. Majority of the inputs are same (A and C). So a a different value for B is not causing any problem. So it could could be said that, majority voter works properly in such faulty hardware condition.

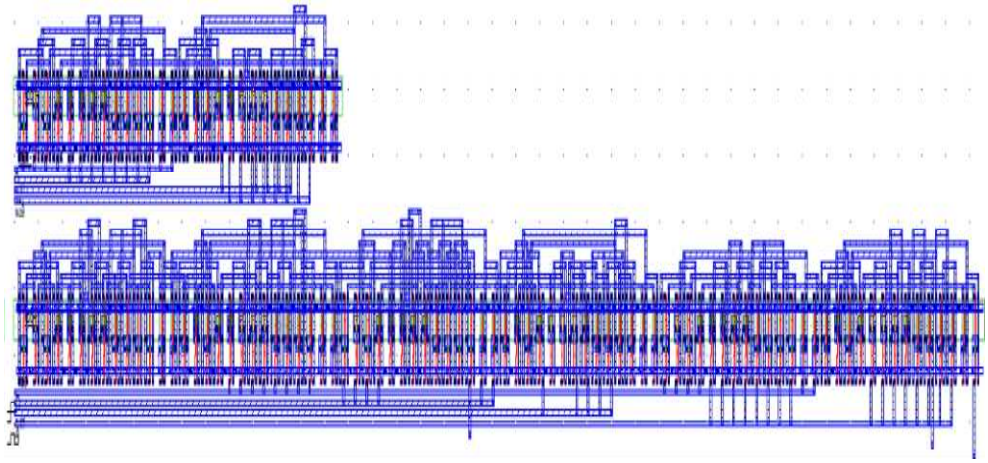

***Figure 10.*** *Voter Circuit affected with stuck at 0 problem.*

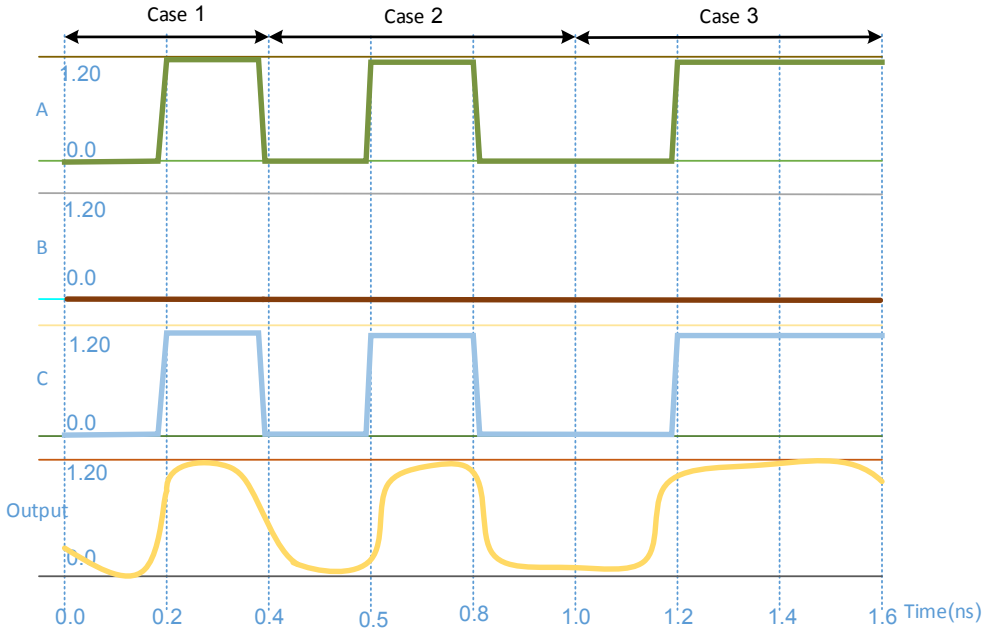


***Figure 11.*** *Output of Voter circuit affected with struck at 0 defect.*

*Testing with stuck at 1 fault*

Double–stuck short or their corresponding bridge defects are tolerated as long as they do not occur to any series transistors. Figure 12 shows the structure of voter circut with stuck at 1 fault and corresponding output is shown in Figure 13. From the output of Figure 13 it is seen that, input A is stuck at 1 for the whole time period. But input A and B are same. So, just like a correct voter circuit, proposed voter

structutre is following B and C, thus giving correct result.

Like same way, proposed voter circut has been tested with different fasulty condition, but it works properly in presence of such hardware faults and defects.

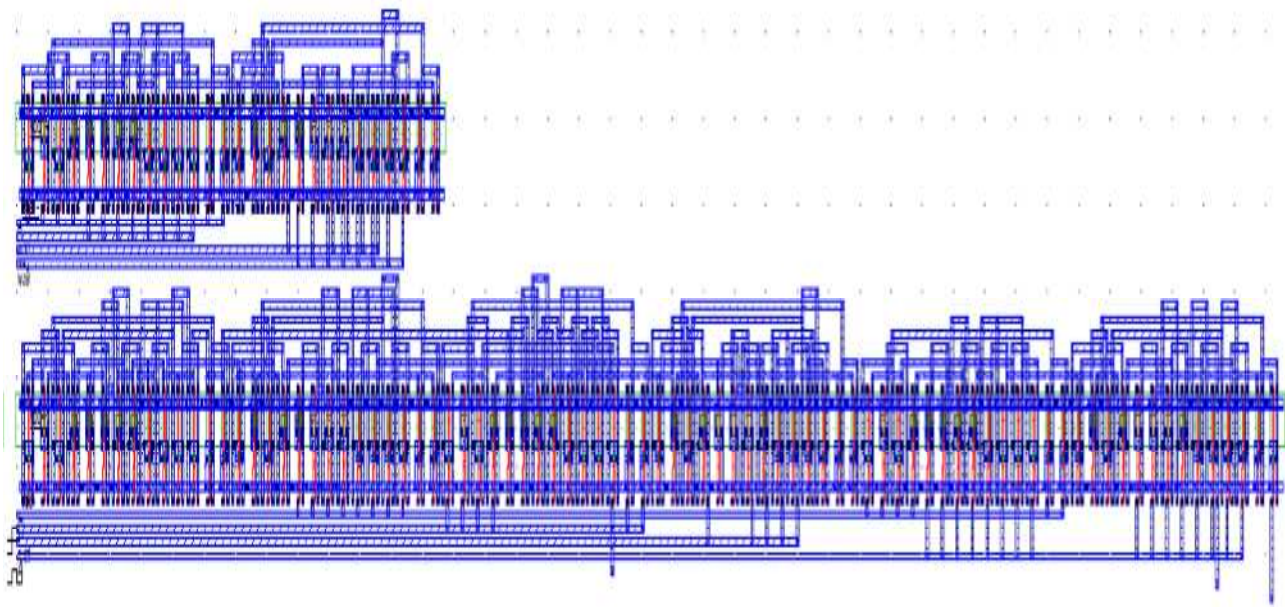

***Figure 12.*** *Voter Circuit affected with stuck at 1 problem.*

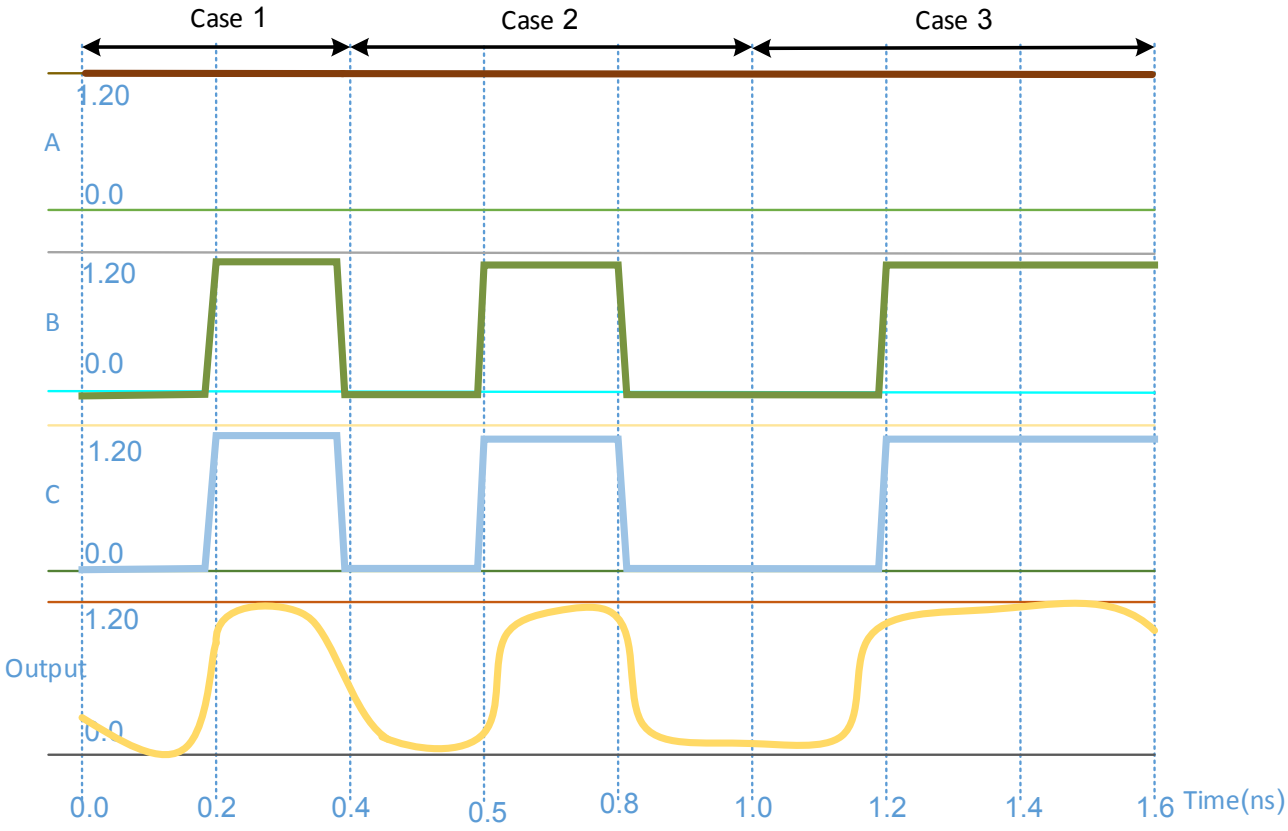


***Figure 13.*** *Output of Voter circuit affected with struck at 1 defect.*

## 5. Discussion

The FPNI architechture provides combined shrinkage of field programmable arrays. Simulation shows that, the approach is highly defect tolerant usually occuring in nanoscale structures. According to our simulation results, FPNI can simultaneously improve three performance issues with respect to CMOSonly FPGAs: circuit density, power, and defect tolerance, without requiring improvements in the

transistors themselves. Variations in nanowire and junction electrical properties will present challenges in modelling ultimate device performance—it is likely that the power and clock rate will be need to be determined empirically for each chip. the extremely high switch redundancy in FPNI, shown in in the defect-tolerance experiments, can be exploited to make compilation viable in a reasonable amount of time. Scaling down both nano and CMOS fabrication dimensions causes dynamic power dissipation to scale down as well, primarily due to reduced wire capacitance from shorter wires. Unfortunately, static power dissipation in CMOS increases as feature sizes decrease, and nanowire resistance increases rapidly as cross-sectional area shrinks, causing RC delays to reduce performance. Circuit designers at the nanoscale will be forced to make trade-offs between clock rate, area, power, and fabrication cost.

# 6. Conclusion

Nano scale devices, assembled chemically or lithiographically, must face high probability of failure. Any Nano scale architechtures built from huge numbers of nanoscale devices contain a huge number of defects. So, it's a great challenge for the engineers to develop such fault tolerant architechture. Redundancy techniques such as N-tuple modular redundancy (NMR) is now widely used to correct faulty behavior and achieve high reliability. NMR systems require a voter in order to decide the final output. But if the voter circuit itself is faulty, then the circuit becomes unreliable. So, a fault tolearble voter circuit is in need for such redundancy techniques. In this research work, a quaded structure NAND gate using four transistor is proposed. Using this quaded structure NAND, a triple modular redundancy (TMR) based voter circuit for fault tolerant nano architechture is proposed.

To evaluate the effectiveness of the voter circuit an IC layout in 90nm CMOS technology is developed. FPNI layout using qNAND hypercell is also designed and analysed. By simulation procedure it has been shown that the proposed fault tolerant voter circuit works properly as a majority voter in different faulty conditions of a TMR system. Moreover, it has been shown that in the presence of internal hardware failure (failure in transistor level) the voter circuit works properly. This voter circuit can be used for fault tolerance purposes in any redundant architechtures efficiently.

# References

[1] O. Ruano, J. A. Maestro, P. Reviriego, "A Methodology for Automatic Insertion of Selective TMR in Digital Circuits Affected by SEUs," IEEE Transactions on Nanotechnology, vol.56, Issue 4, pp. 441-451, Aug. 2009.

[2] J. Vial, A. Bosio, P. Girard, "Using TMR Architectures for Yield Improvement," in IEEE International Symposium on Defect and Fault Toleranceof VLSI Systems, DFTVS, pp.7-15, Oct. 2008.

[3] D. M. Blough, G. F. Sullivan, "A comparison of voting strategies for faulttolerant distributed systems," in IEEE symposium on Reliable Distributed Systems, pp. 136-145, Oct. 1990.

[4] A. Namazi, S. Askari and M. Nourani, "Highly reliable A/D converter using analog voting," in IEEE International Conference on ComputerDesign, pp. 334-339, Oct. 2008.

[5] R. V. Kshirsagar, R. M. Patrikar, "Design of a novel fault-tolerant voter circuit for TMR implementation to improve reliability in digital circuits," in Microelectronics Reliability, vol.49, pp.1573-1577, Dec. 2009.

[6] Tian Ban and Lirida A. B. Naviner, "A Simple Fault-tolerant Digital Voter Circuit in TMR Nanoarchitectures", IEEE International NEWCAS Conference, Montreal, Canada 2010-06

[7] F. L. Kastensmidt, L. Sterpone, L. Carro, and M. S. Reorda. On the Optimal Design of TripleModular Redundancy Logic for SRAM-based FPGAs. Proceedings of Design, Automation and Test in Europe, pages 1290–1295, 2005.

[8] N. Rollins,M. Wirthlin, P. Graham, and M. Caffrey. Evaluating TMR Techniques in the Presence of Single Event Upsets. Proceedings of 6th Annual International Conference onMilitary and Aerospace Programmable Logic Devices (MAPLD), May 2003.

[9] R. Hentschke, F. Marques, F. Lima, L. Carro, A. Susin, and R. Ries. Analyzing Area and Performance Penalty of Protecting Different Digital Modules with Hamming Code and Triple Modular Redundancy. Proceedings of the 15th Symposium on Integrated Circuits and Systems Design, page 95, September 2002.

[10] Chen He, Margarida F. Jacome, and Gustavo de Veciana, "A Reconfiguration-Based Defect Tolerant Design Paradigm for Nanotechnologies," IEEE Design & Test of Computers, July–August 2005, pp. 316–326.

[11] S. Spagocci and T. Fountain, "Fault Rates in Nanochip Devices," Proc. Electrochemical Society, 1999, vol. 98–19, pp. 582–593.

[12] Darshan D. Thaker, Francois Impens, Isaac L. Chuang, Rajeevan Amirtharajah, and Frederic T. Chong, "Recursive TMR: Scaling Fault Tolerance in the Nanoscale Era," IEEE Design & Test of Computers, July–August 2005, pp. 298–305.

[13] R. Iris Bahar, "Trends and future directions in nano structure based computing and fabrication," International Conference on Computer Design (ICCD 06), pp. 522–528, 2006.

[14] Huang, C, "Robust Computing with Nano-Scale Devices, Progress and challenges," Springer, 2010.

[15] J. Vial, A. Bosio, P. Girard, "Using TMR Architectures for Yield Improvement," in IEEE International Symposium on Defect and Fault Tolerance of VLSI Systems, DFTVS, pp.7-15, Oct. 2008.

[16] Snider, Gregory S., and R. Stanley Williams. "Nano/CMOS architectures using a field-programmable nanowire interconnect." Nanotechnology 18.3 (2007): 035204.

[17] Kule, Malay, Hafizur Rahaman, and Bhargab B. Bhattacharya. "Reliable logic design with defective nano-crossbar architecture." Distributed Computing, VLSI, Electrical Circuits and Robotics (DISCOVER), IEEE. IEEE, 2016.

[18] Altun, Mustafa, Valentina Ciriani, and Mehdi Tahoori. "Computing with nano-crossbar arrays: Logic synthesis and fault tolerance." 2017 Design, Automation & Test in Europe Conference & Exhibition (DATE). IEEE, 2017.

[19] Altun, Mustafa, Valentina Ciriani, and Mehdi Tahoori. "Computing with nano-crossbar arrays: Logic synthesis and fault tolerance." 2017 Design, Automation & Test in Europe Conference & Exhibition (DATE). IEEE, 2017.

[20] Kanvitha, P., and N. Naga Raju. "FAULT SECURE ENCODER AND DECODER FOR NANO-MEMORY APPLICATIONS." (2016).