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An Optimized DAC Timing Strategy in SAR ADC with Considering the Overshoot Effect

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Abstract: In this paper, we report an ultra-low power successive-approximation-register (SAR) analog-to digital converter (ADC) by using a DAC timing strategy with considering overshoot effect to increase the sampling rate. This ADC is simulated for power supplies voltage of 0.6 V and 1.2 V in a 130-nm CMOS technology. The results indicate an ENOB greater than 9.3 bits for its full sampling-rate range (4 to 32 MS/s) with an FOM=5.3 to 9.3 fJ/conv-step.

Keywords: Data Converter, Overshoot Effect, Asynchronous Process, Power Efficiency, DAC Timing Strategy, Low Power Designs

1. Introduction

The SAR converters (ADCs) with a medium resolution (8 to 10 bits) and medium frequencies (a few tens to hundreds of MS/s) is one of the applications used in wireless networks and digital TV where small area, low power consumption and high sampling rate in single channel SAR are necessary [1, 2]. Thanks to technology scaling, the problem of long conversion time has been alleviated in these structures. The sampling rate is decreased with increasing the circuit resolution due to serially produce of the output bits. In order to increase the speed of SAR ADCs, different techniques have been recently reported such as multi-bit/step [3], time interleaving [4, 5] and the non-binary search algorithms [6]. Another appropriate method for speed up the sampling rate is the use of asynchronous process [7, 8]. S.W.M. Chen and et al. have proved that the maximum asynchronous conversion time is half of that in its synchronous counterpart [7]. Furthermore, the asynchronous process saves some area and power because it removes the need for some internal clock generator circuit.

In this work, to improve the speed of the converter with high power efficiency, a new approach to asynchronous processing by considering the overshooting effect is proposed which compared to the conventional method. A 10-bit 4-32 MS/s SAR ADC has been applied for investigation of the proposed asynchronous process on its speed.

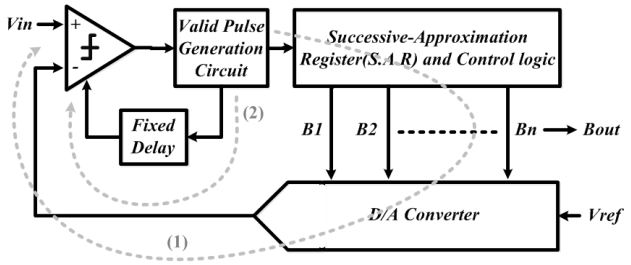
The paper is organized as follows: section 2 briefly describes the conventional asynchronous process of the converter and its challenges; section 3 provides the details of the proposed asynchronous process and its circuit level implementation. The effectiveness of the target asynchronous process method compared to its conventional counterpart is also discussed in this section. Section 4 shows the effectiveness of the proposed asynchronous process technique by using extensive simulation results in 130nm digital CMOS process. Finally, in section 5, we conclude.

2. Conventional Asynchronous SAR ADC

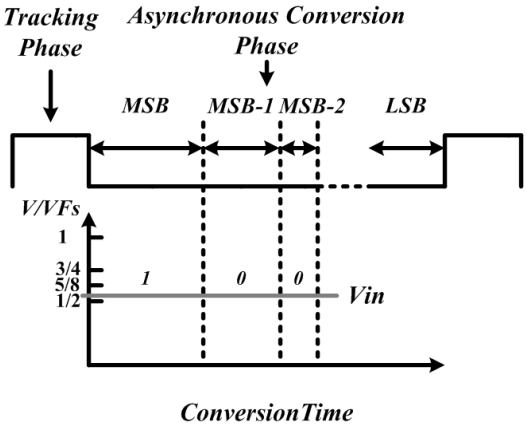
Fig. 1 shows the block diagram of the SAR ADC based on the asynchronous process and the corresponding clock phases. As can be seen from path 2 in Fig. 1(a), a control signal (Valid) is produced by the comparator to confirm that the next clock cycle may start when the comparator's output is ready. On the other hand, the next clock cycle cannot start because the SAR logic and the DAC not generate the next comparison voltage at the input of the comparator as seen path 1 in Fig. 1(a). Consequently, this valid signal of path 2 needs a fixed delay before going to the comparator. For the total conversion phase using the asynchronous process, in average, less time are required as mentioned in [7]. In a conventional asynchronous process, the SAR logic delay and worst-case delay of the DAC settling time determine this fixed delay.

The ADC clock frequency strongly depends on the DAC settling time since the pulse width dedicated to each DAC

capacitor as explained in [8]. Consequently, two design options for the DAC switching can be used in order to reduce the total DAC settling time as follows: 1) utilizing the same size switches with low equivalent resistance for all bits in the DAC in order to have a fast settling response; and 2) equalizing the settling time from MSB to LSB with scaled switches [8]. The DAC settling time decreases from MSBs to LSBs when the settling accuracy is designed to be the same for all bits. Since the step voltage is small, the pulse width dedicated for settling of LSB capacitors can be reduced to achieve higher speed.



(a)



(b)

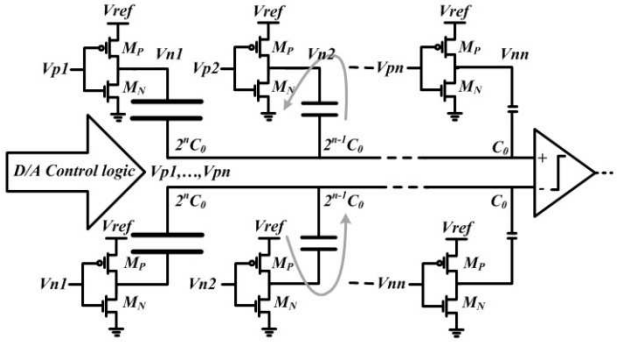
Fig. 1. *(a)Architecture of the conventional asynchronous SAR ADC (b) Conventional asynchronous process timings.*

3. The Proposed Asynchronous SAR ADC

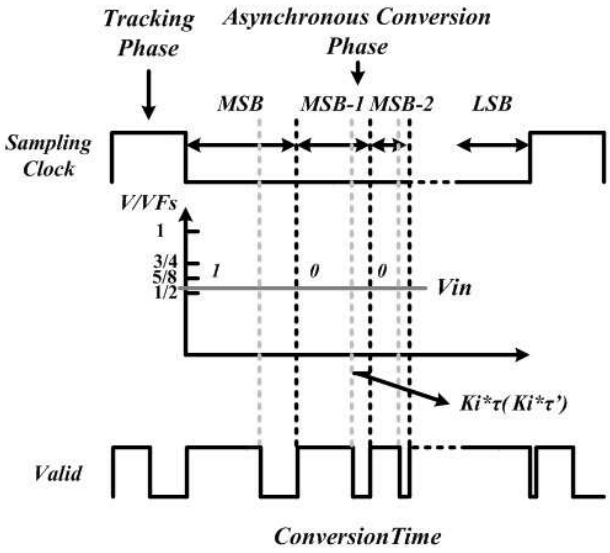
3.1. Architecture

The *fixed delay* is determined based on the worst-case delay required for the DAC settling time in a conventional asynchronous SAR ADC as mentioned in the previous section. Since the settling times for each of the D/A array capacitors are different, the settling time can be reduced with switching of the DAC array. Therefore, the delay in path 2 of Fig. 1(a) reduces with moving from MSB to LSB capacitors. Consequently, the total A/D conversion time reduces. Thus, the delay in path 2 of Fig. 1(a) can be reduced when moving from MSB to LSB capacitors, and, hence, the total A/D conversion time can be reduced.

Fig. 2 shows the schematic of proposed SAR structure in asynchronous conversion phase and its asynchronous process approach, where, τ_i and k_i are the time constant and accuracy of DAC settling for the DAC capacitor C_i, respectively. The architecture of Fig. 1(a) can be changed to Fig. 3 according to what was mentioned above. In this figure, two types of delay in the clock generation path considered as follows: 1) the fixed delay in order to the new decision requirements to be prepared by the control logic circuitry; 2) variable delay for the D/A array capacitors settling.



(a)



(b)

Fig. 2. *(a)Schematics of the SAR ADC in asynchronous conversion phase (the cycle associated with generating the (MSB-1) bit) (b) Proposed asynchronous process approach.*

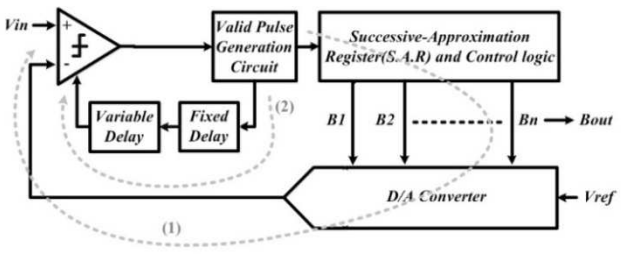


Fig. 3. *Architecture of the proposed asynchronous SAR ADC.*

3.2. Circuit Implementation

The circuit implementation and the timing diagram of the proposed asynchronous clock generator are presented in Fig. 4. The signal delay associated with the OR gate and the internal delay associated with the buffer chain causes fixed and variable delays, respectively. Due to utilizing the unary delay line, the buffer chain has a good accuracy.

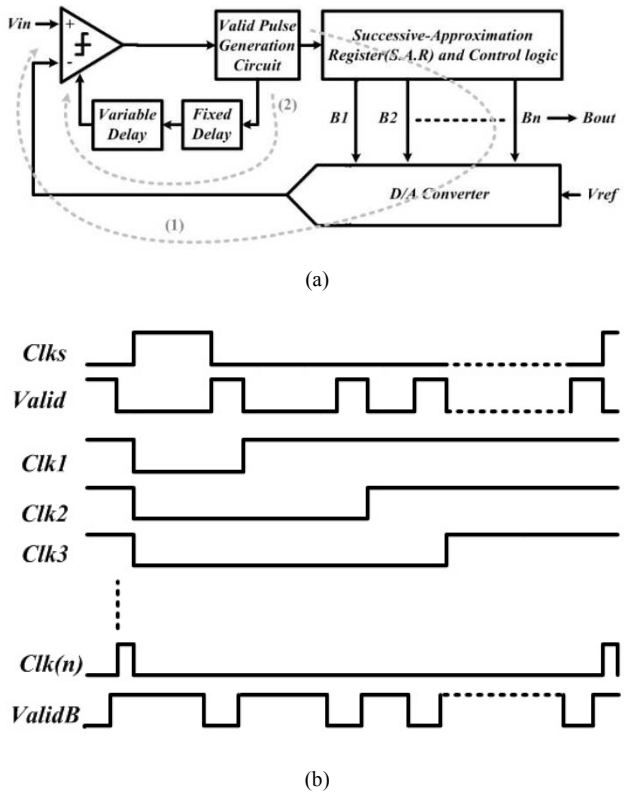


Fig. 4. *(a)Proposed asynchronous clock generator circuit (b) proposed asynchronous clock generator timing curves.*

Each buffer includes two cascaded inverters with the same sizes and power supply voltages that cause the same delay. In order to eliminate buffer delay and reduce the power of the delay line, a reset terminal is utilized for each buffer. Therefore, the total power consumption of the ADC reduces. Since resetting the buffer causes its output be zero, the input of the OR gate associated with this buffer output will be zero and the delay signal generated will be reduced. As depicted in Fig. 4, the conventional asynchronous clock generator make the reset signal required for the buffer line that additional circuit are not required.

As shown in Fig. 4, the operation of the asynchronous clock generator circuit is as follows: each buffer is active at the comparison phase and its output becomes 'high' until the reset signal is applied. Since each buffer in the chain has a specific delay and the outputs of the buffers are connected to an n-input OR gate, resetting each buffer causes reduction of the delay signal, which is called the *Valid B* here, generated by the OR gate.

The 2^n buffers in the chain are required to produce the bits from MSB to LSB in the case of an *n-bit* asynchronous SAR ADC with unary delays. Therefore, the size and power consumption of the clock generator circuit increases drastically. Moreover, the switches in Fig. 2(a) provide an overshoot when the D/A voltage changes due to their gate-drain capacitance. The D/A array capacitors transfer the switches overshoot to the D/A array capacitors output which increases the capacitive settling time. The effect of overshoot is more on less significant bits since the overshoot is the same for different capacitances [9]. Therefore, it is necessary not to dedicate very small settling time to the less significant bits capacitors of the D/A array compared with MSBs capacitors. According to the number of the SAR ADC output bits, the number of buffers is set. Also, the total delay of the buffer chain can be designed based on the settling time of the MSB capacitor. Consequently, with eliminating each buffer from the chain, the total delay of the chain is reduced for different D/A capacitor. However, R. Sekimoto and et al. have recently reported a binary delay line which is proportional to D/A array settling time that the delay line has controlled with a separate circuit and consume extra power [10]. Also, no time has dedicated results some errors in the comparator decision for the overshoot effect and making the new decision.

4. Simulation Results

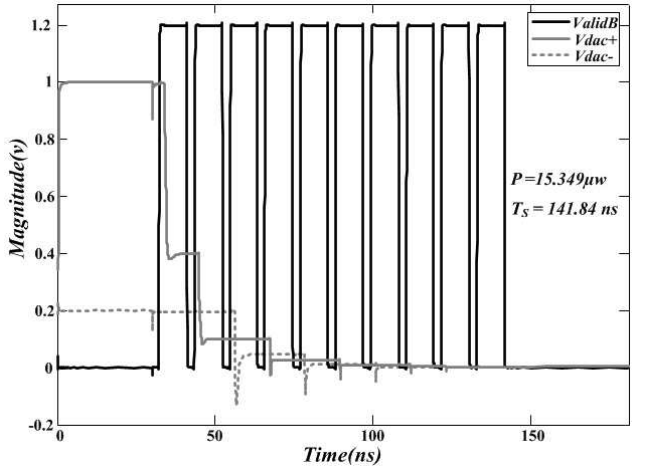
The proposed asynchronous clock generator and logic control circuit have been optimized for power consumption and area. The simulation results are presented as follows:

4.1. Time Domain Performance

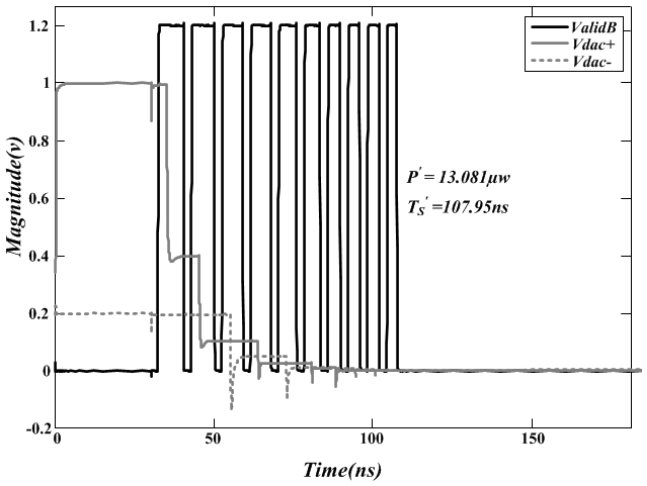
Fig. 5 shows the comparison of the power dissipation and conversion time of proposed 10-bit 4-MS/s SAR ADC with conventional 10-bit 4-MS/s SAR ADC with a monotonic capacitor switching procedure has been implemented. As seen, the difference in the dedicated pulse width to the D/A capacitive array between the conventional and the proposed asynchronous process has been investigated. All of the SAR ADC conditions are the same for two structures but in the conventional one, none of the chain buffers are reset unlike the proposed one. Therefore, both the power dissipation and the conversion time are more compared to the proposed one.

4.2. Dynamic Performance

Fig.6 demonstrates the FFT spectrum with an input frequency of close to nyquist rate and a 4-MS/s sampling rate for power supplies voltage of 0.6 V and 1.2 V. Its SNDR and SFDR are 58.2 dB and 67.4 dB, respectively. The simulated ENOB, FOM and power dissipation values of the proposed SAR versus the input frequency at 4 MS/s are presented in the Fig. 7. The simulated ENOB and power dissipation are about 9.3 bits and 13.7 μw at input frequency close to 0.5MHz, respectively. Since the level shifters were unable to charge the D/A array capacitors, the maximum FOM is 6.8 fJ/step-conv at 0.1 sampling rate.



(a)



(b)

Fig. 5. Comparison of the conversion time and power dissipation between (a) Conventional (b) Proposed 10-bit 4-MS/s SAR ADC with a monotonic capacitor switching procedure.

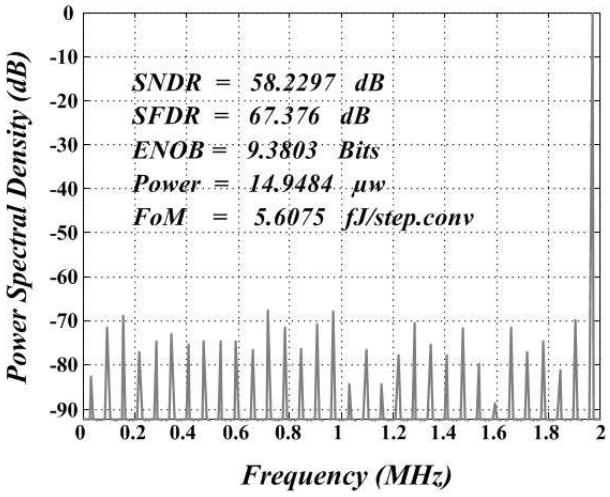
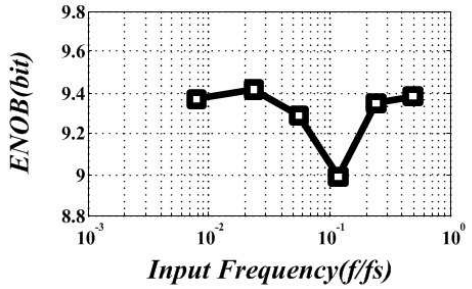
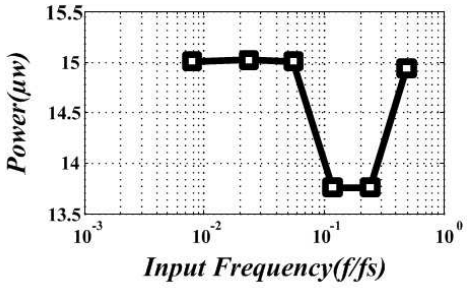


Fig. 6. Simulated 2,048-point FFT spectrum at 4-MS/s.



(a)



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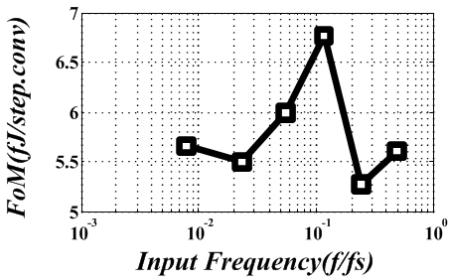

(c)

Fig. 7. The parameters (a) ENOB (b) FoM (c) Power dissipation of the SAR ADC versus input frequency at 4-MS/s.

Table 1. *Simulated dynamic performance at different corners.*

Corners	Dynamic Performance			
	SFDR(dBc)	ENOB(bit)	Power(µw)	FoM(fJ/c-s)
T.T	69.365	9.348	13.758	5.277
S.S	66.528	9.357	13.900	5.301
F.F	65.277	9.192	15.622	6.676

Table 2. *Specification summary versus sampling frequency.*

Specification Summary	Sampling Frequency			
	4	8	16	32
ENOB(Bits)	9.35	9.38	9.41	9.28
Power(µw)	13.76	31.17	59.74	185.80
FoM(fJ/c-s)	5.28	5.86	5.50	9.35
V_{DDL} (v)	0.6	0.6	0.75	1.2
V_{DDH} (v)	1.2	1.2	1.2	1.2

The simulated ENOB and Power Dissipation were about 9.4 bits and 15 µw, respectively, when the input frequency was decreased or increased to 0.5 MHz. Therefore, resultant FOM is about 5.5 fJ/step-conv.

Table 3. *Comparison Summary to State-of-the-Art Works.*

Specification	Papers					
	JSSC'10 [1]	**ESSCIRC'11 [10]**	**ISSCC'12 [12]**	**MWSCAS'13 [13]**	**JSSC'12 [14]**	***This Work***
Technology(nm)	130	40	90	130	40	130
Supply Voltage(V)	1.2	0.6&0.7	1.1	1.2	0.5	0.6&1.2
Sampling Rate(MS/s)	50	8.2	4	64	1.1	4
Resolution(Bits)	10	10	10	10	8	10
DAC unit Capacitor(fF)	4.8	0.5	0.6	5.5	0.5	1
ENOB(Bits)	9.2	7.7	9	8	7.5	9.35
Power(μw)	826	21.5	17.4	1325	1.2	13.76
FOM(fJ/c-s)	29	12.5	8.5	78.7	6.3	5.3

For the different process and temperature corners, all the simulations results of the 10-bit 4-MS/s SAR ADC have been summarized in Table I. Also, the simulated performances versus the sampling frequency with a 1-MHz sinusoidal stimulus are shown in Table II. The ENOB was still higher than 9 bits at sampling rate of 32 MS/s. Since the conversion time was insufficient, further increasing the sampling rate rapidly degraded the performance. The maximum sampling rate was limited to 32MS/s in our proposed SAR ADC due to the low supply voltage has been used for digital circuitry and asynchronous clock generator resulting in more delay times for digital circuits. As seen, reducing the sampling frequency (in this case up to 4MS/s) does not noticeably affect the performance.

4.3. Comparison and Discussion

In order to compare the proposed ADC to previous experimental results with different sampling rates and resolutions. At 4 MS/s and 0.6-V, 1.2-V supplies, the well-known figure-of-merit (FOM) equation [1] is used. The FOM of the proposed ADC is 5.3 fJ/conversion-step at 4 MS/s and 0.6-1.2 V supplies. Also, the FOM is 9.28fJ/conversion-step for 32 MS/s sampling rate. Table III compares the proposed ADC with other state-of-the-art previous experimental results [1], [10], [12], [13]-[14]. As can be seen from Table III, the proposed ADC has the lowest FOM compared to those of previous results with similar sampling rates and resolutions however it was simulated using 130-nm CMOS technology.

5. Conclusion

A new approach to asynchronous processing was proposed for extremely low power SAR ADC. Compared to the conventional method, it can further increase the speed of the converter with high power efficiency. The proposed circuit achieves a 4-32 MS/s operation speed with power consumption of between 14-186μW, resulting in a FOM of 5.3 fJ/conversion-step. The results indicate that proposed SAR ADC can has higher speed and power efficiency.

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