

A design solution to reduce DC bus voltage stress in single switch power quality converter

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To cite this article:

Bindu S. J., C. A. Babu. A Design Solution to Reduce DC Bus Voltage Stress in Single Switch Power Quality Converter. *Journal of Electrical and Electronic Engineering*. Vol. 2, No. 5, 2014, pp. 75-81. doi: 10.11648/j.jeee.20140205.11

Abstract: Power quality is becoming an important issue for electricity consumers at all level of usages. Sensitive equipment and non-linear loads are common in both industrial and domestic environment. Harmonic distortion can result in malfunction of sensitive equipments and generators. Power factor corrected converter is increasingly used in industry to improve input current quality and regulate the output voltage of front end converter. This paper presents a Single Switch Power Quality Converter which achieves both power factor correction and output voltage regulation by using only one switch. This paper deals with the design method in the reduction of DC bus voltage stress during light load, by selecting proper boost inductor using Equal Area Criterion (EAC).

Keywords: Power Factor Correction, BIFRED Converter, Equal Area Criterion, Power Quality, DC Bus Voltage Stress

1. Introduction

Electronic equipments are increasingly being used in everyday life nowadays. A power converter is used as an interface between utility and most of the power electronic equipments. Since these converters draw pulsed current from the supply, which is high in third and fifth harmonic content, line current harmonics are injected to the electrical network. Hence, a power factor correction (PFC) stage is usually inserted to the existing equipment to shape the line current into a sinusoidal waveform and to satisfy necessary standards such as IEEE 519[1] and EN 61000-3-2 [2]. Another reason to limit harmonic currents is to use the full rated current from the available power source. The goal then of a PFC converter is to reduce the harmonic content of the current waveform and keep the phase angle between the current and the voltage as small as possible. In effect the circuit wants to emulate a resistive load.

The new generation of power factor corrected single stage power supplies typically takes the form of a cascaded combination of Discontinuous Conduction Mode (DCM) PFC converter and a DC-DC converter. The two converters share the same controller and switch to regulate the output voltage and to shape the input current. In order to buffer the difference between the instantaneous input power and constant output power an energy storage element is required [3].

Several single stage power factor correction converters have been previously proposed such as Boost Integrated with Fly Back Rectifier / Energy storage / DC- DC (BIFRED) converter which is the integration of a Discontinuous Conduction Mode (DCM) boost converter with Continuous Conduction Mode (CCM) fly back converter. Here DCM boost converter is for input current wave shaping and CCM fly back dc-dc converter is for isolation and load voltage regulation.

Disadvantage of Single Switch power quality converter is that it usually suffers from relatively higher voltage stress at light load [3], [4]. The reason for high DC bus voltage stress during light load is the power unbalance between PFC stage and output stage. Many methods for reducing voltage stress have been reported. One of the proposed solutions for overcoming the dc bus voltage stress is using frequency control [5]. But this approach has short comings which lead to increase in component count and making the control circuit more complex. Another solution proposed; is the concept of series charging and parallel discharging capacitor scheme [6]. The disadvantage of this method is that it increases the number of components in the power circuit. Another approach to this problem is by modulating the predetermined operating frequency of the converter [7]

which results in increased complexity in the control circuit. Two elements are common in the design of single switch power quality converter. First, the mode of input inductor must be maintained such that input inductor begins and ends each switch cycle at a ground state. Second, the converter must have an energy storage capacitor which is capable of providing energy when the instantaneous line voltage is near zero.

Fig 1 shows BIFRED converter with negative feedback in the power stage. When Switch S is made ON, the rectified voltage is applied to inductor L_i and the inductor current linearly increases. Therefore, during the ON time interval of the switch, the inductor stores energy independently. When switch S is made OFF, the stored energy of the inductor L_i is transferred to, capacitor C_b and the load. The input power is controlled only by duty cycle and L_i . The PFC stage really does not know whether the load is low or high. So during light load, the energy stored by the PFC stage is same as that of the heavy load causing power unbalance between the input and output [1]. The bulk capacitor stores this unbalanced power leading to increase in the dc bus voltage. If the PFC stage is inherently able to reduce the input power automatically when the load becomes light, then the dc-bus

voltage can be suppressed. One approach to this problem is using proper closed loop controller, which will work in such a way that error between reference voltage and output voltage will be zero, by reducing the ON time interval of the switch, thus maintaining the power balance. Another method is to reduce the voltage across L_i during the switch ON time period, so that the energy absorbed from the line input is also reduced [2].

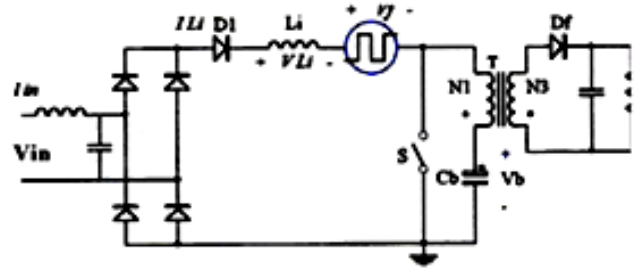


Fig 1. BIFRED Converter with negative feedback in the power stage

2. The Proposed Single Switch Power Quality Converter

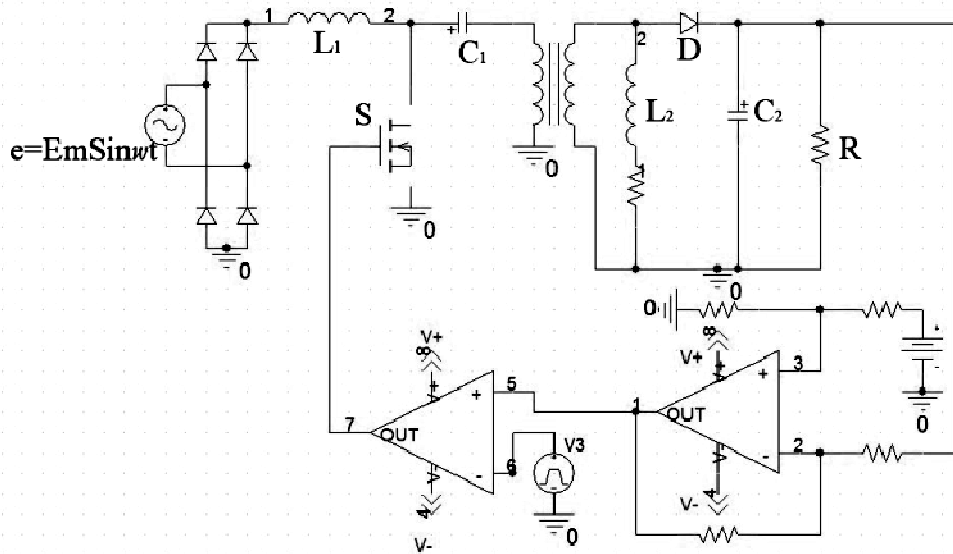


Fig 2. The Proposed Single Switch Power Quality Converter

Proposed converter, shown in Fig. 2, is a BIFRED converter, which eliminate diode D_1 and the use of power circuit negative voltage feedback V_f . We should consider the diode D_1 only if the EMI filter is used after the full bridge rectifier. In order to eliminate the problem of DC bus voltage stress at light load, Equal Area Criterion (EAC) is applied for the optimum design of boost inductor and a proportional controller, with duty ratio as manipulated variable and output voltage as controlled variable. To fully explain the circuit, converter operation will be analyzed according to the three operational intervals.

The first interval starts when the switch S turns ON, the input voltage is applied across the inductor. Depending upon the input voltage, energy will be stored in L_1 and Diode D is

reverse biased.

The second interval starts when S turns OFF, which causes the current in inductor L_1 to ramp down and Diode D conducts.

The third interval starts when the current in inductor L_1 remains zero, S remains OFF and Diode D conducts. Load receives energy from the coupled inductor L_2 , and C_2 passes energy to the load.

DC bus voltage is eliminated by the selection of inductance using Equal Area Criterion (EAC) along with a proportional controller, by selecting boost inductor in such a way that it should store the energy that matches with the energy required at the output during light load. Here EAC is applied in each switching cycle by equating the area under

the inductor current and the area under the reference current. For the design of boost inductor, it is considered that maximum power is delivered at the peak value of input voltage and the duty ratio will be slightly less than 0.5 for maximum power delivery. EAC is applied between theoretical value of input current and the peak inductor current at maximum turn ON time.

3. Design of Power Factor Correction Stage Using EAC

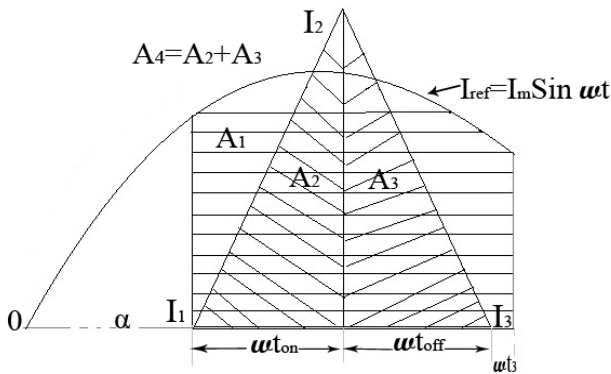


Fig 3. Reference current superimposed on inductor current pulse

Time period $T = t_{on} + t_{off} + t_3$
 ωt_{on} - switch on period.
 ωt_{off} - switch off period.
 ωt_3 - dead period
 Consider,
 α -Angle of switching instant

EAC applied to PFC converter means equalizing the area under the inductor current and the area under sinusoidal reference current over one switching cycle [8]. The reference current $I_m \sin \omega t$ superimposed on the current through the inductor over a switching interval is shown in Fig. 3. Anticipating sinusoidal input current at unity power factor, an input current is obtained. Peak value of input current during t_{on} is calculated at peak value of sinusoidal reference current.

$$\omega t_{on} + \omega t_{off} + \omega t_3 = \theta \tag{1}$$

3.1. EAC for the Design

The area A_1 under the reference current $I_m \sin \omega t$ in one switching cycle is given by

$$A_1 = \int_{\alpha}^{\alpha+\theta} I_m \sin \omega t \, d\omega t \tag{2}$$

$$A_1 = -I_m [-\cos(\alpha + \theta) - \cos \alpha] \tag{3}$$

When $\alpha = 90^\circ$,

$$A_1 = I_m \sin \theta \approx I_m \theta \tag{4}$$

since θ is very small.
 Area A_4 is a triangle

$$\text{Therefore } A_4 = A_2 + A_3 = \frac{1}{2} [\omega t_{on} + \omega t_{off}] I_{2\text{peak}} \tag{5}$$

Current through the boost inductor during ON period is given by

$$E_m \sin \omega t = L_1 \, di/dt \tag{6}$$

$$i = \int \frac{E_m}{L_1} \sin \omega t \, dt \tag{7}$$

Current through the boost inductor during OFF period is given by

$$L_1 \, di/dt = E_m \sin \omega t - [V_{dc} + nV_2] \tag{8}$$

$$i = \int \frac{E_m}{L_1} \sin \omega t \, dt - \frac{V_{dc} + nV_2}{L_1} dt \tag{9}$$

When switch is ON instantaneous current is given by,

$$i_r = I_1 + \frac{E_m}{\omega L_1} [\cos \alpha - \cos(\alpha + \omega t)] \tag{10}$$

Here, $\alpha < \omega t < \omega t_{on}$

When switch is OFF instantaneous current is given by,

$$i_r = I_2 + \frac{E_m}{\omega L_1} (\cos \alpha + \alpha_{on}) - \cos(\alpha + \alpha_{on} + \omega t) - \frac{(V_{dc} + nV_2)}{\omega L_1} \omega t \tag{11}$$

At the beginning $I_1 = 0$

During on time,

$$i_r = \frac{E_m}{\omega L_1} [\cos \alpha - \cos(\alpha + \omega t)] \tag{12}$$

Where $\alpha < \omega t < \omega t_{on}$

Off mode current becomes zero at $\omega t = \omega t_{off}$

$$I_2 = I_2 + \frac{E_m}{\omega L_1} [\cos(\alpha + \alpha_{on}) - \cos(\alpha + \alpha_{on} + \omega t)] - \frac{(V_{dc} + nV_2)}{\omega L_1} \omega t$$

$$\text{Where } \alpha < \omega t < \omega t_{off} \tag{13}$$

3.2. Design Consideration of Boost Inductor

The value of this inductor is quite crucial in the performance of the converter, with the small value of this inductor the large switching ripples are injected into supply current, and large value of it doesn't allow shaping the AC mains current in the desired fashion. Therefore the optimum selection of this inductor is essential to achieve satisfactory performance [9].

Design Basis:

- 1 Assuming zero switching loss.
- 2 Required power output is obtaining at a low turn ON time or duty ratio (0.26), by this varying power levels can be achieved under DCM.
- 3 Find out value of input peak current during turn ON such that area under reference input current in one

switching period made equal to the area under the current pulse as shown in fig. 3

4 Switching instance is considered as $\alpha = 90^\circ$ for the maximum rising and falling slope at the peak of input voltage.

Maximum current (I_{2peak}) occurs at the end of ON duration.

Using EAC, we have,

$$A_1=A_4 \tag{14}$$

Hence from (4) & (5)

$$I_m \theta = \frac{1}{2}[\omega t_{on} + \omega t_{off}] I_{2peak} \tag{15}$$

Select reference current in such that-

$$P_{out} = V_{rms} \times I_{rms \cdot ref} \tag{16}$$

From I_{rms} we can find I_m

And using (15) we get the value for I_{2peak} .

Select L_1 such that I_{2peak} occurs maximum duty cycle and $\alpha = 90^\circ$. The OFF duration followed by this I_{2peak} will be minimum and the current at the end of this off duration is zero.

From (12)

$$I_{2peak} = \frac{E_m}{\omega L_1} \sin \omega t_{on} \tag{17}$$

$\sin \omega t_{on} \cong \omega t_{on}$, due to high switching frequency.

$$I_{2peak} = \frac{E_m}{\omega L_1} \omega t_{on} = \frac{E_m}{L_1} t_{on} = \frac{E_m}{L_1} DT \tag{18}$$

$$L_1 = \frac{E_m}{I_{2peak}} DT \tag{19}$$

Here D represents duty cycle

3.3. Expression of DC Bus Voltage, Output Voltage and Duty Ratio

From (13), (17) with $I_3=0$ and assuming $\omega t_3 \cong 0$

$$0 = I_{2peak} + \frac{E_m}{\omega L_1} (-\sin \alpha_{on} + \sin \alpha_{on} + \omega t_{off}) - \frac{(V_{dc} + nV_2)}{\omega L_1} \omega t_{off} \tag{20}$$

$$0 = \frac{E_m}{\omega L_1} (\sin \alpha_{on} - \sin \alpha_{on}) + \frac{E_m}{\omega L_1} \sin(\alpha_{on} + \omega t_{off}) - \frac{(V_{dc} + nV_2)}{\omega L_1} \omega t_{off} \tag{21}$$

We have $\sin \omega t_{on} \cong \omega t_{on}$, due to high switching frequency

$$\frac{(V_{dc} + nV_2)}{L_1} t_{off} = \frac{E_m}{L_1} (t_{on} + t_{off}) \tag{22}$$

$$(V_{dc} + nV_2)(t - t_{on}) = E_m T \tag{23}$$

Where $T=t_{on}+t_{off}$,

$$(V_{dc} + nV_2)t - (V_{dc} + nV_2)t_{on} = E_m T \tag{24}$$

$$\frac{t_{on}}{T} = \frac{(V_{dc} + nV_2 - E_m)}{(V_{dc} + nV_2)} \tag{25}$$

$$D = 1 - \frac{E_m}{(V_{dc} + nV_2)} \tag{26}$$

Where $D = \frac{t_{on}}{T}$,

$$V_{dc} + nV_2 = \frac{E_m}{1 - D} \tag{27}$$

4. Design Example of Single Switch Power Quality Converter

Converter with the following specification is designed:

Input Supply Voltage = 230 V, 50Hz

Output Voltage $V_{dc} = 50$ V

Output power = 100W

Switching frequency $f_s = 20$ KHz

Output voltage ripple = 5 %

Duty ratio of the switch = 0.26

4.1. Determining Value of ' L_1 ' Using EAC

Consider $\alpha = 90^\circ$, as the switching instant

$$D = 0.26$$

Switching frequency $f_s = 20$ KHz

From (19),

$$L_1 = 1.57 \text{mH}$$

4.2. Determining Value of Energy Storage Capacitor

The value of DC bus voltage capacitor is quite crucial as it affects the response, cost, stability, size and efficiency. A small value of the capacitor results in large ripple in steady state and big dip and rise in dc link voltage under transient condition. A high value of it reduces the DC bus voltage ripple but increases cost, size, and weight.

From (19) we have,

$$I_{peak} = \frac{DTE_m}{L_1}$$

Energy Stored in inductor = $\frac{1}{2} L_1 I_{2peak}^2$

Energy Stored in capacitor = $\frac{1}{2} C_1 V^2$

$$C_1 V^2 = L_1 I^2$$

$$C_1 = 116\mu F$$

5. Control Scheme

Control is necessary for the regulation of output voltage and for improvement of line harmonics. Straight forward duty ratio control is a suitable method of output voltage regulation, due to its simplicity of design using conventional PWM circuitry. Proportional controller is used here, using duty cycle as the manipulated variable, and output voltage as the controlled variable.[10]

6. Simulation Results

To investigate and validate the design the proposed converter was simulated using SABER. The results were found in accordance with the design intends.

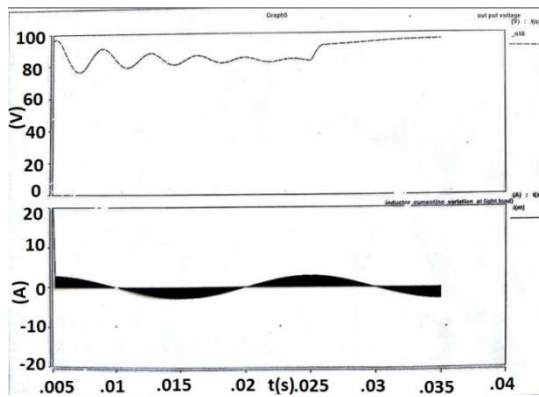


Fig.4. Output voltage and input current under open loop

Open loop simulation was carried out by varying the duty ratio. Output voltage is found linear to ON duty ratio. Input current is sinusoidal and in phase with the input line voltage. Effect of sudden decrease in output load on dc bus voltage was studied. Fig 4 shows that during open loop when load is reduced after 25 ms there is a slight increase in the output voltage, no variation in the input current. Fig.4 also shows that the input converter draws the same current under varying load condition.

Performance under closed loop condition was studied by varying the reference voltage. Output voltage was found varying linear with the reference voltage and input current was found sinusoidal and in phase with the input voltage.

Fig.5 shows the load transient response, the transient overshoot voltage is less than 1%. Fig. 6 shows variation in input line current when the load is reduced after 15 ms. It is observed that in closed loop condition the dc bus voltage stress has been drastically reduced. When output load is decreased suddenly, instantaneous power unbalance will occur, causing the output voltage and dc bus voltage to increase. Proportional controller will immediately detect the increase in output voltage and takes the corrective action by reducing the duty cycle leading to a new energy balance within one to two switching cycles. Fig 7 shows the voltage across switch when load thrown out at 15ms and also we can

observe that the corrective action started within 2 switching cycle, which conform the fast transient response. Fig 8 shows plot between dc bus voltage stress on energy storage capacitor and output power, which confirms the effectiveness in the reduction of dc bus voltage stress. The proposed converter can keep the capacitor voltage between 217-230V for a load change of full load to 10% of load.

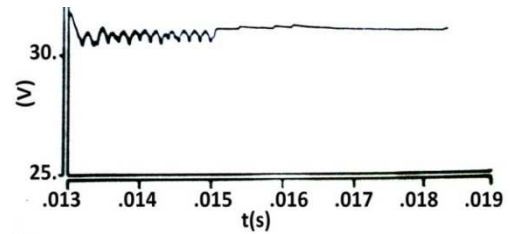


Fig 5. output voltage under closed loop

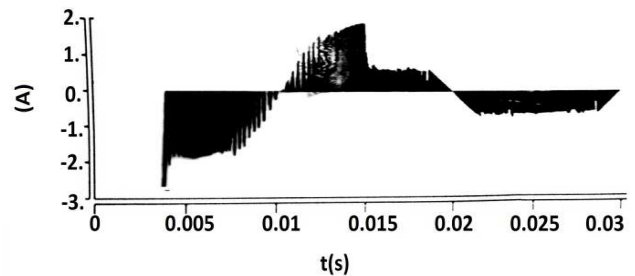


Fig 6. Input current under closed loop

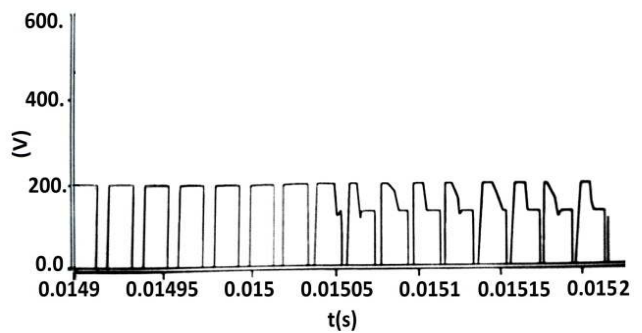


Fig 7. voltage across switch when load thrown out at 15ms

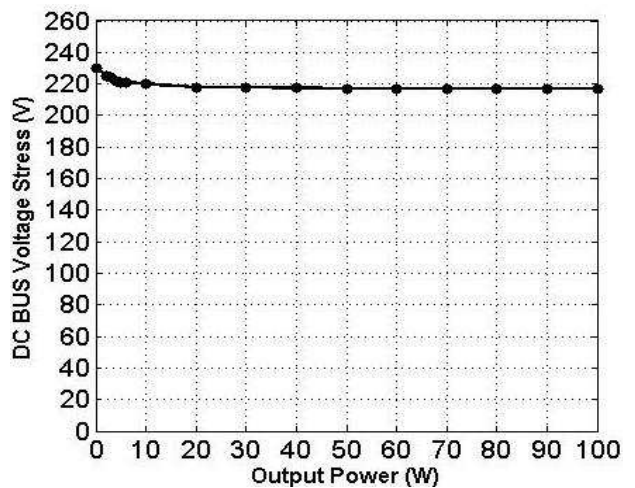


Fig 8. Measured DC Bus voltage Stress against output power

Table I. Measured Harmonic Currents Versus EN Requirements

Harmonic Order n	Measure harmonic Current (mA) @ $I_{line}=6.27A$	Extrapolated harmonic Current(mA) @ $I_{line}= 6A$	Maximum Permissible current(mA) of EN 61000-3-2
3	60.6	1441	2300
5	18.18	432	1140
7	12.1	288	770
9	8.1	193	400
11	6.5	155	330
13	5.8	138	210
15	5.3	126	150

Table I reveals that proposed converter can provide sufficient margin in harmonic current reduction, even if at line current of 16 A.

7. Experimental Verifications

In order to verify the circuit operation, a 100W, 50V output voltage PFC converter was implemented at constant switching frequency of 20KHz and tested with the following circuit parameters and using MOSFET IRFPF50 as switch. Fig.9 shows input voltage and dc bus voltage. Fig.10 shows input line current is sinusoidal and in phase with the input voltage. The power factor was found to be closed to unity.

Table II. Specifications And Components For The Single Switch Power Quality Converter

Parameter	Value
L_1	1.57mH
C_1	116 μ F
n	3.5
C_2	317 μ F
T_s	50 μ s
D	0.26
R	25 Ω
S	IRFPF50
L_1 Core	E 42/21/15
L_1 Winding	116T,13 Wires of SWG 30
Transformer Core	E 65/32/13
Transformer L_2	1.2 mH
Primary Winding	297 T ,SWG 21
Secondary Winding	99 T, SWG 18

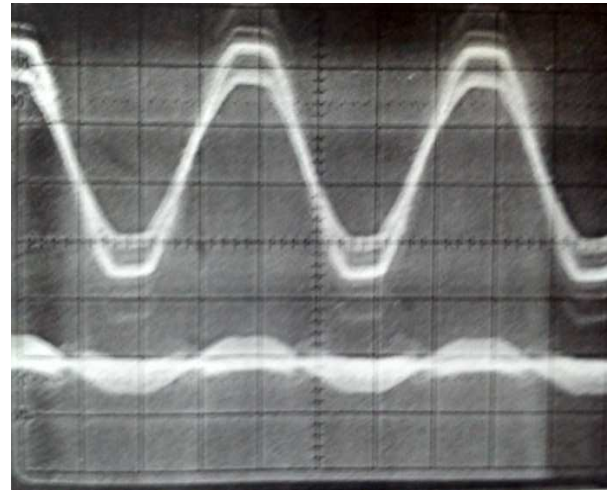


Fig. 10. Input voltage and input current

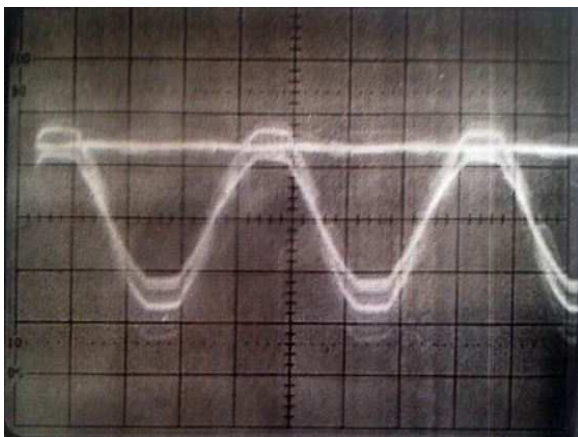


Fig 9. Input voltage and DC bus Voltage

8. Conclusion

This paper derives a design solution for achieving low voltage stress and unity power factor, in a Single Switch Power Quality converter by optimally selecting the boost inductance using EAC. Fast voltage regulation is achieved by simple PWM control. The performance of the converter with the proportional controller has been verified. The limiting duty ratio for the normal operation of the proposed converter is 0.5. It is observed that by proper selection of the inductance using EAC and with the simple proportional controller, the DC bus voltage at light load is found completely eliminated.

The proposed converter has a simpler power circuit and simpler control circuit, has less component count, and it does not contribute to any additional voltage stress. For cost sensitive application this converter may be preferred.

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