Journal of Electrical and Electronic Engineering
2013; 1(5): 107-113
Published online November 30, 2013 (http://www.sciencepublishinggroup.com/j/jeee)
doi: 10.11648/j.jeee.20130105.11

Design and Analysis of a 0.4V 1.08mW 12GHz High-Performance VCO in 0.18μm CMOS (Invited Paper)

To-Po Wang, Chung-Chin Li

Department of Electronic Engineering and Graduate Institute of Computer and Communication Engineering, National Taipei University of Technology, Taipei, Taiwan, R.O.C

Email address:
tpwang@ntut.edu.tw (T. P. Wang)

To cite this article:
To-Po Wang, Chung-Chin Li. Design and Analysis of a 0.4V 1.08mW 12GHz High-Performance VCO in 0.18μm CMOS (Invited Paper). *Journal of Electrical and Electronic Engineering*. Vol. 1, No. 5, 2013, pp. 107-113. doi: 10.11648/j.jeee.20130105.11

Abstract: This paper presents the design and analysis of a high-performance fully-integrated 0.18μm CMOS voltage-controlled oscillator (VCO) with low supply voltage and low dc power consumption. To enhance the transconductance (g_m) of MOSFETs and negative conductance ($-G_m$) of a cross-coupled pair, the device size of the nMOS cross-coupled pair is enlarged. For reducing the supply voltage and minimizing the dc power consumption, forward-body biased technique is utilized in this VCO, leading to the threshold voltage (V_t) reduction. Moreover, process variations are taken into accounted at low supply voltage, and the Monte-Carlo analysis is used to analyze the VCO phase noise and output power. At 0.4V low supply voltage, the fabricated 0.18μm CMOS VCO consumes 1.08mW low core power. At this bias condition, the measured phase noise at 1MHz offset from 12.77GHz carrier is -110.2 dBc/Hz, and the measured tuning range is 5.75%. Compared to recently published 0.18μm X-band CMOS VCOs, this work demonstrates the low supply voltage, low dc power dissipation, superior figure-of-merit (FOM), and better figure-of-merit including the tuning range (FOM_T).

Keywords: Monte-Carlo Analysis, Negative Conductance, Transconductance,Voltage-Controlled Oscillator

1. Introduction

With the rapid development of high-speed wireless communication, the requirements of low voltage and low dc power are the trend for circuits. With CMOS feature size advances to deep-submicron range, the CMOS voltage-controlled oscillators with operation frequencies up to X band were reported [1]-[6]. In [1], the cascode CMOS *LC* VCO with Q-enhancement technique for large voltage swing and low phase noise was presented. However, the 1.8V high supply voltage and 8.1mW large core power are required. To solve the transconductance and load mismatch problems of a conventional current-reused VCO for obtaining symmetrical oscillation signals and lowering the phase noise, a modified current–reused configuration consists of two dc level shifts was proposed in [3]. This dc level shifter, however, required 1.8V high supply voltage and 8.1mW large core power. For increasing negative resistance in a VCO, a method of applying additional cross-coupled pair at the VCO core was described in [4]. Although this additional cross-coupled pair can relax the start up condition, however, it raised the total power dissipation up to 16.27 mW. In addition to these difficulties, the accuracies of passive and active devices modeling are needed to be considered [7]-[10].

In this paper, a differential cross-coupled VCO with an oscillation frequency around 12GHz with 0.4V low supply voltage and 1.08mW low core power is presented. At the 0.4V low supply voltage, by increasing the MOSFET device size and utilizing forward-body bias, the negative-conductance of the cross-coupled pair can be effectively improved. In addition, a capacitive-divided feedback is used in this work to boost the output voltage swing, leading to the low phase noise performance.

This paper is organized as follows. In Section 2, the low-voltage low-power CMOS VCO is introduced. The design considerations including the negative-conductance topology, forward-body bias, and capacitive-divided feedback are presented. Section 3 gives the experimental results and characterization. Finally, a conclusion is provided in Section 4.

2. Design and Analysis of Low-Voltage Low-Power VCO

For a regular cross-coupled VCO operating in X band, it has to increase the supply voltage and dc power dissipation for overcoming the difficult startup condition. Moreover, the degraded MOSFET transconductance limits the output voltage swing, leading to a poor VCO performance. To overcome these difficulties, a fully-integrated low-voltage low-power high-performance X-band CMOS VCO is presented in [11], as shown in Fig. 1. The device size of the cross-coupled pair (M_1-M_2) is enlarged (W_1/L_1=W_2/L_2=147μm/0.18μm) to boost the negative conductance ($-G_m$). In addition, forward-body-bias technique is used to reduce the threshold voltage of MOSFETs (M_1-M_4) for low-voltage and low-power operation [12]. Furthermore, the capacitive-divided feedback (C_{DS} and C_S) is connected between drain and source terminals of the devices (M_1-M_2), resulting in increased output voltage swings and improved phase noise. The considerations of designing and analyzing the low-voltage low-power high-performance VCO are presented as follows.

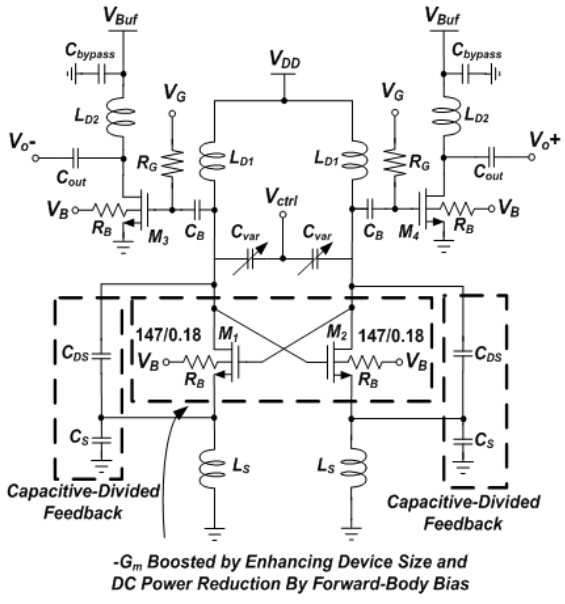

Fig1. *Schematic of the fully integrated low-voltage low-power high-performance X-band CMOS VCO [11].*

2.1. Enhanced Negative Conductance of the Cross-Coupled Pair

To analyze the negative-conductance enhanced cross-coupled pair shown in Fig. 2(a), the bulks of the MOSFETs are connected to supply voltage (V_B) through the current-limited resistors (R_B). From the equivalent half circuit shown in Fig. 2(b), the negative conductance of the cross-coupled pair is formulated as

$$-G_m = \mathrm{Re}\{Y_{IN}\} = -\mu_n C_{OX}\frac{W}{L}\left\{V_{GS}-\left[V_{t0}+\gamma\left(\sqrt{2\phi_f-V_{BS}}-\sqrt{2\phi_f}\right)\right]\right\}. \quad (1)$$

where L is the channel length, W is the channel width, μ_n is the electron mobility, C_{OX} is the oxide capacitance, V_{GS} is the gate-to-source dc bias, V_{t0} is the threshold voltage at V_{BS}=0, γ is a process parameter, and ψ_f is a physical parameter. According to (1), it is observed that an incremental change in body-to-source dc bias (V_{BS}) through the current-limiting resister (R_B) can enhance the negative conductance ($-G_m$).

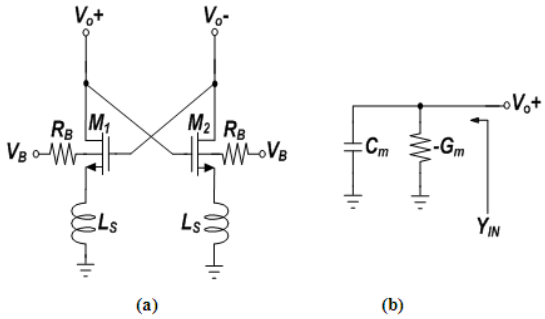

Fig 2. *(a) Negative-conductance enhanced structure and (b) the equivalent half circuit.*

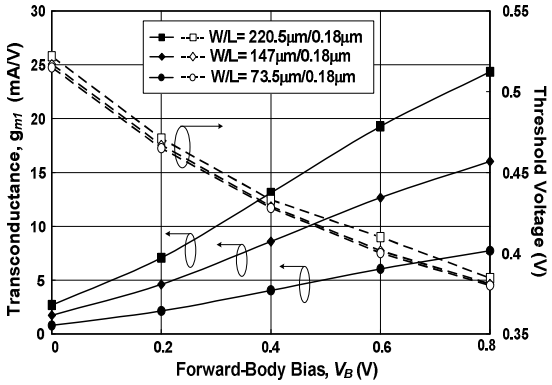

Fig 3. *Simulated transconductance (g_{m1}) and threshold voltage of the MOSFET (M_1) as a function of forward-body bias (V_B) for various transistor sizes.*

The simulated threshold voltage and transconductance (g_{m1}) of the MOSFET (M_1) as a function of forward-body bias (V_B) for various transistor sizes are shown in Fig. 3. From this figure, it is observed that the threshold voltage is reduced from 0.51V to 0.38V, and the transconductance (g_{m1}) is significantly enhanced by raising the forward-body bias (V_B). Fig. 4 shows the simulated drain current and bulk current of the MOSFET (M_1) as a function of forward-body bias (V_B) for various transistor sizes. The bias voltages of the negative-conductance enhanced cross-coupled pair are V_{GS1}=V_{DS1}=0.4V and V_B=0.4V. It is observed that the drain current and bulk current are raised due to the increased forward-body bias (V_B). Therefore, there is a design tradeoff between the transconductance (g_{m1}), drain current, and bulk current. In order to increase the transconductance (g_{m1}) at 0.4V low supply voltage, the design parameters of device

size and forward-body bias are selected as follows: $W_1/L_1=W_2/L_2$=147μm/0.18μm and V_B=0.4V. This 0.4V V_B is much lower than the turn-on voltage of a P-N junction, and the induced bulk current is only 9.5pA. For this reason, the leakage current can be ignored in this design.

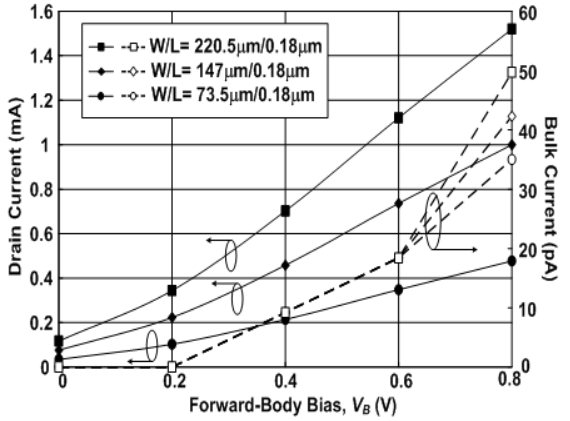

Fig 4. *Simulated drain current and bulk current of the MOSFET (M_1) as a function of forward-body bias (V_B) for various transistor sizes.*

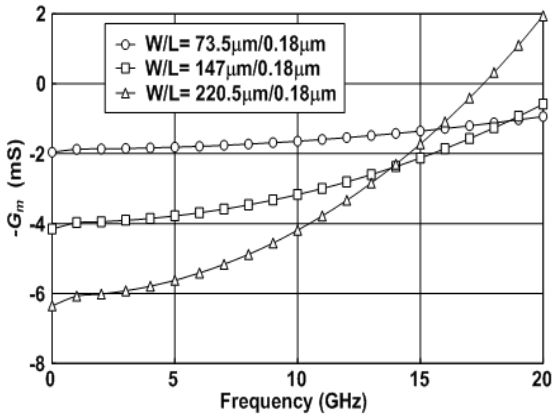

Fig 5. *Simulated negative conductance (-G_m) versus frequency for various transistor sizes.*

From Fig. 3 and Fig. 4, it is observed that the threshold voltage of the MOSFETs (M_1-M_2) used in this VCO can be reduced from 0.517V to 0.429V by increasing the forward-body bias (V_B) from 0V to 0.4V, leading to an 88mV threshold voltage reduction. The raised drain current is from 0.076mA to 0.458mA, and the induced core power is only 0.4V x 0.382mA= 0.1528mW. These result in the measured 0.4V low supply voltage and 1.08mW low dc power dissipation for sustaining VCO oscillation in X band.

To have better understanding of the influences of the enlarged MOSFETs, the simulated negative conductance (-G_m) versus frequency for various transistor sizes is shown in Fig. 5. The bias conditions are V_{GS1} =V_{DS1}=0.4V and V_B=0.4V. From this figure, it is observed that the negative conductance (-G_m) can be enhanced from -1.54mS to -2.81mS at 12GHz because of the increased device size from W/L=73.5μm/0.18μm to W/L=147μm/0.18μm.

2.2. Capacitive-Divided Feedback

Fig. 6 shows the simplified equivalent half-circuit model of the VCO. To simply the analysis procedure, the parasitic capacitances (C_{gs2} and C_{gd2}) are ignored. By utilizing Kirchhoff's current law (KCL) with small signal analysis, it yields

$$V_{S2}=\frac{-s^2L_SC_{\text{var}}V_o}{\left(1+s^2L_SC_S\right)\left(1+s^2L_{D1}C_{\text{var}}\right)} \tag{2}$$

$$V_{S2}=\frac{V_i\left(sL_Sg_{m2}\right)+V_o\left(s^2L_SC_{DS}\right)}{s^2L_S\left(C_S+C_{DS}\right)+sL_Sg_{m2}+1}. \tag{3}$$

Combine (2) and (3), the transfer function considering the V_o and V_i of the active device M_2 can be formulated in (4). From (4), it is observed that the Vo/Vi can be increased by utilizing a small capacitance ratio (C_{DS}/C_S).

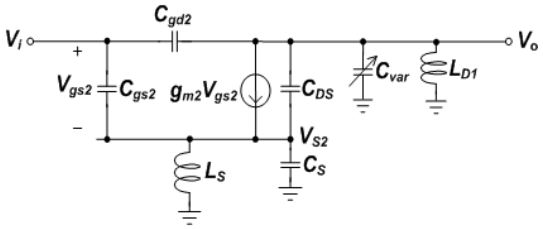

Fig6. *Half-circuit model of the presented VCO.*

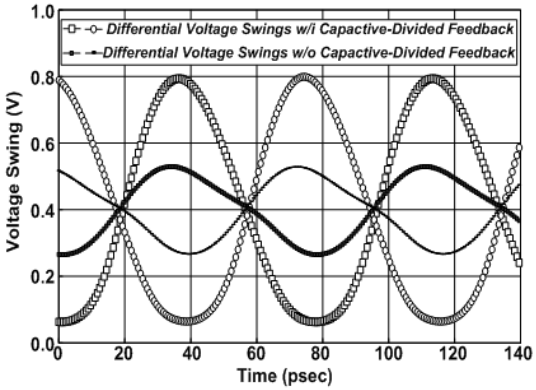

Fig 7. *Simulated differential voltage swings at tank with and without the capacitive-divided feedback.*

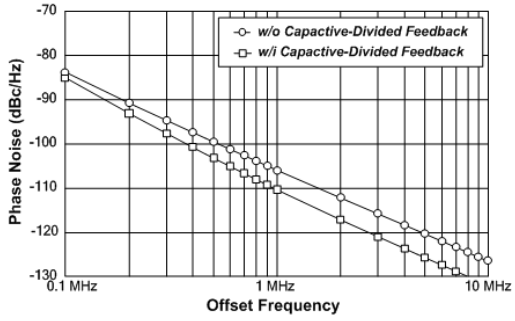

Fig 8. *Simulated phase noise of the 12.77GHz VCO with and without the capacitive-divided feedback.*

Fig. 7 depicts the simulated differential voltage swings of the low-voltage low-power VCO with and without the

capacitive-divided feedback. The capacitance values of the C_{DS} and C_S are 0.1 pF and 0.4 pF, respectively. This leads to a capacitance ratio of 1/4. According to (4), it also predicts that a small capacitance ratio (C_{DS}/C_S) enhances Vo/Vi and VCO loop gain. From Fig.7, it is indicated that the differential voltage swings at the tank with and without capacitive-divided feedbacks are 736 mV_{pp} and 230 mV_{pp}, respectively. Therefore, the voltage swing of a VCO with capacitive-divided feedback is much larger than that of the counterpart. Moreover, the enlarged voltage swings can successfully improve the VCO phase noise due to better impulse sensitivity function (ISF).

In addition, the simulated phase noise of the 12.77GHz VCO with and without the capacitive-divided feedback is shown in Fig. 8. It is clear that the phase noise of the VCO with capacitors (C_{DS} and C_S) can achieve lower phase noise than that of the counterpart because of the boosted voltage swings illustrated in Fig. 7.

2.3. Process Variation Consideration

To consider the VCO properties under a 0.4V low-voltage low-power operation condition, the presented VCO is simulated at different process corners. Table 1 summaries the characterized results at slow, typical, and fast process corners at 0.4V low supply voltage. According to this table, it is indicated that the presented VCO can meet the VCO startup condition at different process corners. Moreover, the VCO tuning range ranges from 5.67% to 5.94%, and VCO phase noise is from -110.74dBc/Hz to -111.11dBc/Hz, and the dc power dissipation is from 0.52mW to 1.97mW.

Table 1. *Simulated VCO performance at different process corner*

ProcessCorner	Slow	Typical	Fast
V_{DD} (V)	0.4	0.4	0.4
V_{ctrl}(V)	-1.0~1.8	-1.0~1.8	-1.0~1.8
Tuning Range (%)	5.94	5.80	5.67
Phase Noise @ 1-MHz offset (dBc/Hz)	-110.74	-111.11	-111.07
DC Power (mW)	0.52	0.99	1.97

In order to characterize VCO output power and phase noise because of the mismatch of the VCO core (M_1-M_2), the Monte-Carlo analysis is adopted to test the VCO. It includes random variations on process parameters of Gaussian distribution. These are channel length, channel width, oxide thickness, and threshold voltage. Fig. 9 depicts simulated results of the output power with Monte-Carlo analysis, comprising a total of 50 sampled data. From this figure, it is observed that the variation of the output power is from -8.422dBm to -8.503dBm, and the maximum discrepancy of these 50 samples is 0.081dB. Moreover, Fig. 10 shows the simulated VCO phase noise with Monte-Carlo analysis, including 50 samples. It is indicated that ranges of the phase noise is from -111.096dBc/Hz to -111.112dBc/Hz, leading to a maximum discrepancy of 0.016dB.

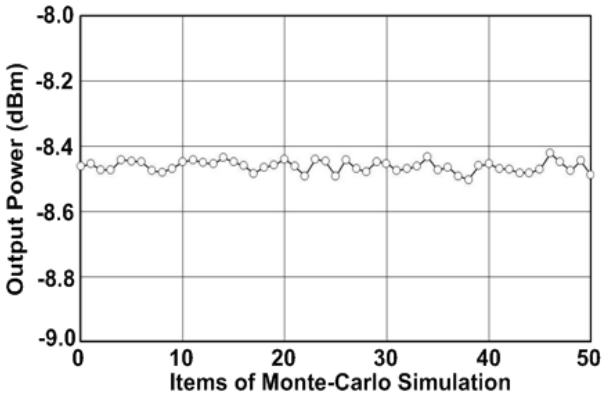

Fig 9. *Simulated output power with Monte-Carlo analysis.*

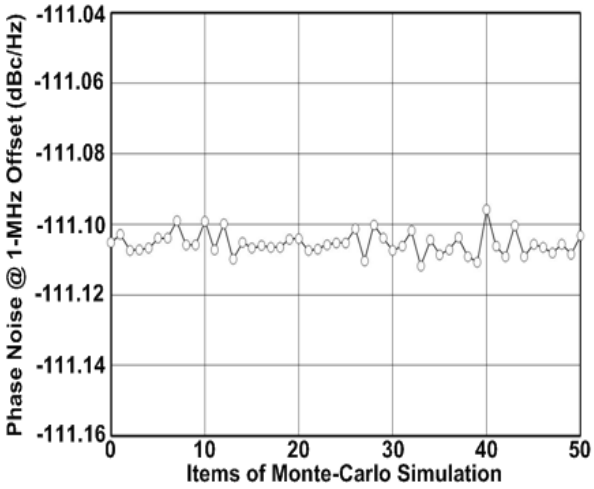

Fig10. *Simulated phase noise with Monte-Carlo analysis.*

$$\frac{V_o}{V_i} = -\frac{g_{m2}\left(s^4 L_S L_{D1} C_{\text{var}} + s^2\left(L_S + L_{D1}\frac{C_{\text{var}}}{C_S}\right) + \frac{1}{C_S}\right)}{s^5 L_S L_{D1} C_{\text{var}} C_{DS} + s^3\left(L_S C_{DS} + L_{D1} C_{\text{var}}\frac{C_{DS}}{C_S} + L_S C_{\text{var}} + L_S\frac{C_{DS}}{C_S}C_{\text{var}}\right) + s^2 L_S\frac{C_{\text{var}}}{C_S}g_{m2} + s\left(\frac{C_{\text{var}}}{C_S} + \frac{C_{DS}}{C_S}\right)}. \quad (4)$$

3. Experimental Results

Fig.11 shows the chip photo of the fabricated VCO in [11] with a chip size of 0.795 × 0.745mm^2. To evaluate the high-frequency performance, the output spectrum and phase noise were characterized by a 50GHz spectrum analyzer. On-wafer probing was used to test the VCO performance. The losses of the measurement setups were de-embedded and calibrated in the experimental results.

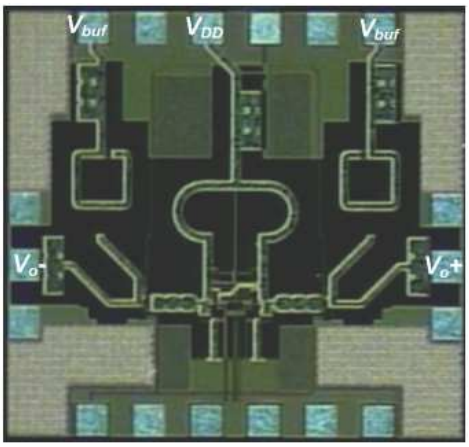

Fig 11. *Chip photoof the fabricated VCO.*

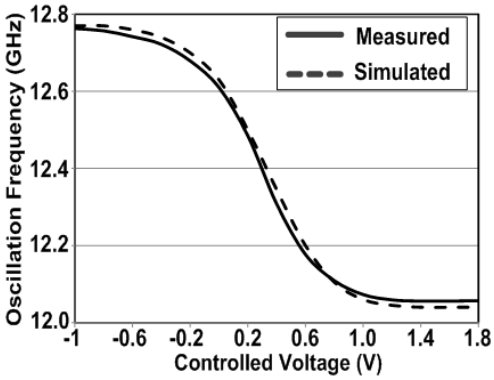

Fig 12. *Characterized oscillation frequency of the fabricated VCO.*

The VCO core consumes 1.08mW from a low supply voltage of 0.4V. Fig.12 shows the characterized oscillation frequency of the fabricated VCO. While sweeping the controlled voltage (Vctrl) from -1V to 1.8V, the VCO exhibits a tuning range of 5.75%. Fig. 13 shows the characterized VCO output power of the fabricated VCO. It is observed that the output power is larger than -10.15dBm covering the tuning frequency. In addition, at this bias condition, the measured phase noise is -110.19dBc/Hz at 1MHz offset from the 12.77GHz carrier, as shown in Fig. 14.

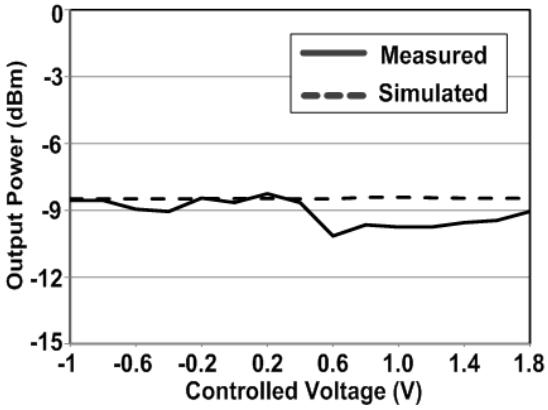

Fig 13. *Characterized output power of the fabricated VCO.*

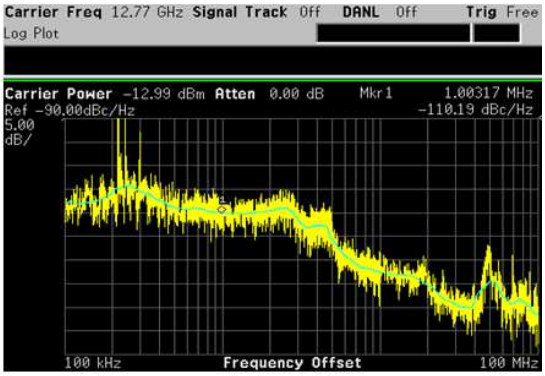

Fig 14. *Measured phase noise of the fabricated VCO.*

Table2. *Performance summary and comparison to the recently published 0.18μm CMOS VCOs around 10 GHz.*

Process	Freq. (GHz)	Tuning Range	Phase Noise @ 1-MHz offset (dBc/Hz)	Core Power (mW)	Supply Voltage (V)	FOM (dBc/Hz)	FOM_T (dBc/Hz)	Ref.
0.18-μm CMOS	11.55	6.22%	-110.8	8.1	1.8	-183.0	-178.8	[1]
0.18-μm CMOS	13.54	7.89%	-112	6.2	1.0	-186.7	-184.6	[2]
0.18-μm CMOS	16	5.6%	-111	8.1	1.8	-186.0	-181.0	[3]
0.18-μm CMOS	10.19	16.10%	-106.19	3	1.5	-181.6	-185.7	[4]
0.18-μm CMOS	13.72	5.9%	-113.8	4.05	0.9	-190.5	-185.9	[5]
0.18-μm CMOS	12.2	3.39%	-112.15	2.18	0.8	-190.5	-181.1	[6]
0.18-μm CMOS	12.77	5.75%	-110.19	1.08	0.4	-192.0	-187.2	this work

Table 2 summarizes the performance of this VCO and compared to the recently published 0.18μm CMOS VCOs around 10GHz. It is indicated that this 12GHz VCO can simultaneously achieve the measured lowest supply voltage (V_{DD}=0.4V) and lowest dc power consumption (P_{DC}=1.08mW) while maintaining low phase noise of -110.19dBc/Hz at 1MHz offset from the 12.77GHz carrier and wide tuning range of 5.75%. In order to characterize the

VCO performance, the widely used figure-of-merit (FOM) [1]-[6], [11], [13] and figure-of-merit including tuning range (FOM_T) [11], [14] are adopted in this work. The FOM and FOM_T are written as

$$\mathrm{FOM} = L(\Delta f) - 20\log_{10}\left(\frac{f_o}{\Delta f}\right) + 10\log_{10}\left(\frac{P_{DC}}{1\mathrm{mW}}\right) \quad (5)$$

$$\mathrm{FOM_T} = L(\Delta f) - 20\log_{10}\left(\frac{f_o}{\Delta f}\cdot\frac{\text{Tuning Range}}{10}\right) + 10\log_{10}\left(\frac{P_{DC}}{1\mathrm{mW}}\right) \quad (6)$$

Where f_o is the carrier frequency, Δf is the offset frequency, $L(\Delta f)$ is the VCO phase noise, and P_{DC} is the dc power consumption. According to table 2, the presented low-voltage low-power VCO achieves the impressed FOM and FOM_T.

4. Conclusion

In this paper, the design and analysis of a high-performance fully-integrated 0.18μm CMOS voltage-controlled oscillator (VCO) with 0.4V low supply voltage and 1.08mW low dc power consumption is presented in detail. The capacitive-divided feedback is used to improve the VCO output voltage swings and phase noise. Moreover, the enlarged MOSFET devices of the cross-coupled pair are adopted to increase the negative conductance ($-G_m$). Furthermore, the forward-body-bias technique is utilized to reduce the supply voltage and dc power dissipation. In addition, the Monte-Carlo analysis is applied to characterize the low-voltage low-power VCO at different process corners.

Acknowledgements

This work is supported in part by the National Science Council of Taiwan, R.O.C., under Contract NSC 99-2622-E-027-031-CC3, NSC 100-2119-M-027-001, NSC 100-2221-E-027-091, NSC 102-2623-E-027-004-NU and NSC 102-2119-M-027-002, and by the National Nano Device Laboratories under Contract NDL 99-C07M2-056. The authors would like to thank the National Chip Implementation Center (CIC), Hsinchu, Taiwan, for chip fabrication, and the National Nano Device Laboratories (NDL), Hsinchu, Taiwan, for measurement support.

References

[1] B. Park, S. Lee, S. Choi, and S. Hong, "A 12-GHz fully integrated cascode CMOS LC VCO with Q-enhancement circuit,"IEEE Microw.and Wireless Compon.Lett., vol. 18, pp.133-135, Feb. 2008.

[2] X. S. Chen, Y. T. Chen, and H. R. Chuang, "A 1-V low-voltage 12-GHz VCO in 0.18-μm CMOS technology," in Asia Pacific Microw. Conf. Tech. Dig., Dec. 2008, pp. 1-4.

[3] C. L. Yang and Y. C. Chiang, "Low-phase-noise and low-power CMOS VCO constructed in current-reused configuration,"IEEE Microw.and Wireless Compon.Lett., vol. 18, pp.136-138, Feb. 2008.

[4] M. T. Hsu and C. T. Chiu, "A low-power 10-GHz current reused VCO using negative resistance enhancement technique," in Asia Pacific Microw. Conf. Tech. Dig., Dec. 2010, pp. 2276-2279.

[5] H. K. Chiou and S. C. Chen, "Low-phase-noise Ku-band Gm-Boosting differential Colpitts VCO," in Asia Pacific Microw. Conf. Tech. Dig., Dec. 2009, pp. 313-316.

[6] S. L. Jang, Y. K. Wu, C. C. Liu, and J. F. Huang, "A dual-band CMOS voltage-controlled oscillator implemented with dual-resonance LC tank,"IEEE Microw.and Wireless Compon.Lett., vol. 19, pp. 816-818, Dec. 2009.

[7] B. Razavi, "Design of millimeter-wave CMOS radios: a tutorial," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 56, no. 1, pp. 4-16,Jan. 2009.

[8] J. Yang, C. Y. Kim, D. W. Kim, and S. Hong, "Design of a 24-GHz CMOS VCO with an asymmetric-width transformer,"IEEE Trans.Circuit and Systems Part-II Express Briefs, vol. 57, no. 3, pp. 173-177, March 2010.

[9] A. Bevilacqua, F. P. Pavan, C. Sandner, A. Gerosa, and A. Neviani, "Transformer-based dual-mode voltage-controlled oscillators,"IEEE Trans.Circuit and Systems Part-II Express Briefs, vol. 54, no. 4, pp. 293-297, April 2007.

[10] N. T. Tchamov, S. S. Broussev, I. S. Uzunov, and K. K. Rantala, "Dual-band LC VCO architecture with a fourth-order resonator,"IEEE Trans.Circuit and Systems Part-II Express Briefs, vol. 54, no. 3, pp. 277-281, Mar. 2007.

[11] T. P. Wang and C. C. Li, "A 0.4-V 1.08-mW 12-GHz high-performance VCO in 0.18-μm CMOS," in 2012 IEEE Radio and Wireless Symposium (RWS) Proceedings, Santa Clara, CA, USA, Jan. 15-18, 2012. pp.207-210.

[12] T. P. Wang, "A low-voltage low-power K-band CMOS LNA using dc-current-path split technology,"IEEE Microwave and Wireless Component Letter, vol. 20, pp.519-521, Sept. 2010.

[13] T. P. Wang, Z. M. Tsai, K. J. Sun, and H. Wang, "Phase-noise reduction of X-band push-push oscillator with second-harmonic self-injection technique," IEEE Trans.Microw. Theory Tech., vol. 55, no. 1, pp.66-77, Jan. 2007.

[14] T. P. Wang, "A fully integrated W-band push-push CMOS VCO with low phase noise and wide tuning range," IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control, vol. 58, no. 7, pp. 1307-1319, July 2011.

Biography

To-Po Wang received B.S. degrees in mechanical engineering and in electrical engineering from National Sun Yat-Sen University, Taiwan, R.O.C., in 1998, the M.S. degree in communication engineering from National Chiao Tung University, Hsinchu, Taiwan, R.O.C., in 2000, and the Ph.D. degree in communication engineering from National Taiwan University, Taipei, Taiwan, R.O.C., in 2007.

His research interests are in the areas of RF and millimeter-wave integrated circuits (ICs) in CMOS, SiGeBiCMOS, and compound semiconductor technologies. He is currently as an Associate Professor.

Chung-Chin Li received the M.S. degree at the graduate institute of computer and communication engineering, National Taipei University of Technology, Taiwan, R.O.C.

His research interests include the design of RF integrated circuits (RFICs).